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Speed Up Li-ion Battery Charging and Reduce Heat with a Switching PowerPath Manager

by Steven Martin

Introduction

Designers of handheld products race to pack as many "cool" features as possible into ever smaller devices. Big, bright color displays, Wi-Fi, WiMax, Bluetooth, GPS, cameras, phones, touch screens, movie players, music players and radios are just a few of the features common in today's battery powered portable devices. One big problem with packing so many features into such a small space is that the "cool" product must actually stay cool while in use. Minimizing dissipated heat is a priority in handhelds, and a significant source of heat is the battery charger.

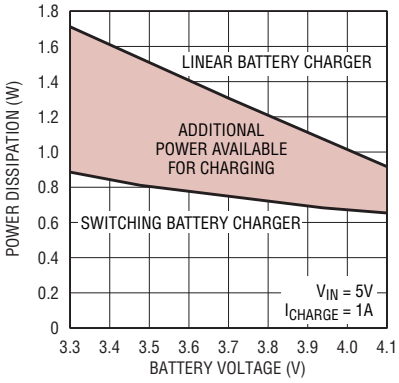

Figure 1. Reduce battery charge time and keep handheld devices cool by using a switching PowerPath manager/battery charger.

One component of handhelds has changed little over the years—the Li-ion battery. While the capacities of today's batteries have increased from a few hundred milliampere hours to several ampere-hours to accommodate the ever expanding feature set of modern portable products, the basic Li-Ion battery technology has remained unchanged. Why has Li-ion survived so long? Unmatched energy density (both by mass and volume), high voltage, low self-discharge, wide usable temperature range, no memory effect, no cell reversal, no cell balancing, and low environmental impact all make the Li-Ion battery the preferred choice for high performance portable products.

Charging today's big batteries, however, is no small deal. In order to charge them in a reasonable amount of time, they should be charged at a rate commensurate with their capacity and with a specific algorithm. For example, to fully charge a 1Ah battery in approximately one hour requires one amp of charge current. If USB powered charging is desired, then only 500mA of current is available, doubling the charge time to two hours.

Another problem with higher charge currents is the additional heat lost in

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Linear in the News...

EDN Innovation Award for Linear Power Device

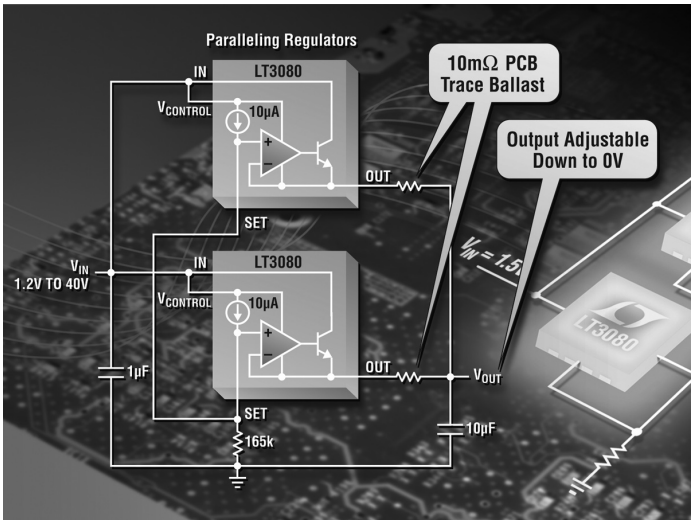
EDN magazine announced the selection of Linear's LT3080 3-terminal parallelable low dropout linear regulator as *EDN's* Innovation of the Year in the Power ICs category. The award was presented at the annual *EDN* Innovation Awards ceremony to Linear Technology Vice President Engineering and Chief Technical Officer Robert Dobkin and Design Engineer Todd Owen, who developed the product. Other Linear Technology finalists included the LTC6102 current sense amplifier in the Analog ICs category, Robert Dobkin for Innovator of the Year, and Jim Williams' article, "Designing instrumentation circuitry with RMS/DC converters" for Best Contributed Article.

According to Ron Wilson, Executive Director of *EDN* Worldwide, "Selected by their peers in the design community for their outstanding results, these innovators stand in the front rank of the best and brightest electronics engineering has to offer."

Robert Dobkin stated, "The LT3080 solves two difficult problems for linear regulators: spreading heat to eliminate heat sinks and increasing output current by simply adding additional devices. The circuit architecture is completely new and just as easy to use as older devices. I am proud to introduce this product."

The LT3080 is a 1.1A 3-terminal linear regulator that can easily be paralleled for heat spreading and higher output current, and is adjustable to zero with a single resistor. This is a new architecture for regulators and uses a current reference and voltage follower to allow sharing between multiple regulators, enabling multiamp linear regulation in all surface-mount systems without heat sinks.

The LT3080 has a wide input voltage capability of 1.2V to 40V, a dropout voltage of only 300mV and millivolt regulation. The output voltage is adjustable, spanning a wide range from 0V to 40V, and the on-chip trimmed reference achieves high accuracy of ±1%.



Hot Products in Asia

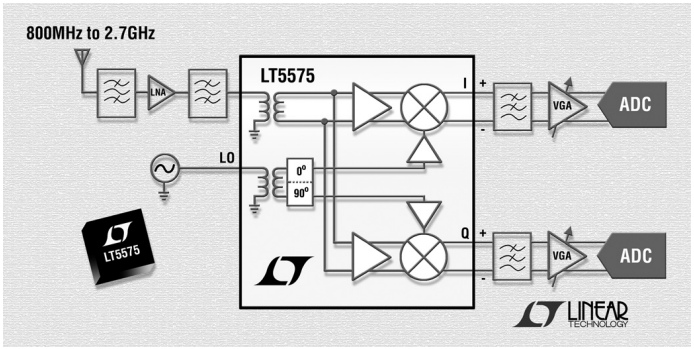
EDN Asia magazine recently announced their list of the 100 Hot Products of 2007. Included in the list are three Linear Technology products:

- ❑ LTC6400 Low Noise, Low Distortion ADC Driver
- ❑ LT4356 Overvoltage Protection Regulator
- ❑ LT3080 3-Terminal Linear Regulator

For more information, visit www.linear.com.

Editor's Choice Award

Portable Design magazine recently announced their selections for their annual Editor's Choice Awards. In the RF/Microwave category, the award went to the LT5575 Direct Conversion I/Q Demodulator. The LT5575, which was also selected by *Electronic Products* magazine as Product of the Year, significantly reduces the cost of 3G



and WiMAX basestation receivers. The LT5575's extended operating frequency range from 800MHz to 2.7GHz covers all of the cellular and 3G infrastructure, WiMAX and RFID bands with a single part. Its capability to convert from RF directly to baseband at DC or low frequency results in simplified receiver designs, reduced component count and use of lower cost, low frequency components.

The LT5575 offers an outstanding IIP3 of 28dBm and IIP2 of 54.1dBm at 900MHz, and an IIP3 of 22.6dBm and IIP2 of 60dBm at 1.9GHz. Moreover, the device has a conversion gain of 3dB, which when combined with a DSB Noise Figure of 12.7dB, produces excellent receiver dynamic range. The device's I (In-phase) and Q (Quadrature phase) outputs have typical amplitude and phase matching of 0.04dB and 0.6°, respectively, providing an unprecedented level of demodulation accuracy.

The LT5575 is capable of supporting multiband basestations covering both the 850MHz GSM/EDGE bands and the 1.9GHz/2.1GHz 3G wireless services (including CDMA2000, WCDMA, UMTS, and TD-SCDMA). It is ideal for single carrier micro- and pico-basestations, where low cost architectures are key. The LT5575's performance is also well suited for 2.6GHz WiMAX basestations, and as an IF demodulator in a microwave radio link or satellite receiver.

LTC4088/LTC4098, continued from page 1

the charging process. Since charge power for these devices usually comes from a 5V source, such as a USB port or 5V wall adapter, power loss can be significant. Assuming a healthy Li-Ion battery spends significant time at its "happy voltage" of 3.7V during charging, then charging efficiency via a linear charging element can at best be 3.7V/5V or 74%. When the battery voltage is less than 3.7V, losses are even worse. Even at the maximum float voltage of 4.2V, where the battery spends about 1/3 of the charge time, charging efficiency can't be better than 84%.

With a 1Ah battery charged at a "1C" rate, we can expect about 1.3W of power to be lost while delivering 3.7W to the battery over the longest part of the charge cycle. Note, however, that the energy delivered to the battery doesn't result in any significant temperature rise as the battery is storing the energy for future use. This means that the predominant source of heat during charging is generated by the charger itself. With this in mind, at a given power level it makes sense to move to a switching battery charger for improved charging efficiency, less charger generated heat and reduced charge time.

Both the LTC4088 and LTC4098 are examples of single-cell Li-ion battery chargers from Linear Technology that not only offer the high efficiency of a switching battery charger but also include PowerPath technology. PowerPath control is a technique that uses a third, or intermediate, node to allow instant-on operation, which provides power to the system when the battery voltage is below the system cutoff. Only products like the LTC4088 and LTC4098 combine a step down DC/DC switching regulator with a linear battery charger in a unique way that ensures high efficiency power delivery to both the system load and the battery. Before we delve into these parts, let's take a look at how it was done before.

Old School: Linear PowerPath

The intermediate node topology isn't new. Figure 2 shows an example of a linear PowerPath topology. In this architecture, a current limited switch delivers power from an input connector to both the external load and linear battery charger. The linear battery charger then delivers power from the intermediate node to the battery.

If the load current is far enough below the input current limit to allow some current to be directed to battery charging, the voltage at V_{OUT} is nearly equal to the input supply voltage, let's say 5V. In this case, the path from V_{IN} to V_{OUT} is extremely efficient since there is no significant voltage drop across the pass element. Note, however, that the voltage drop between V_{OUT} (~5V) and V_{BAT} (say 3.5V) means the linear charger is running inefficiently. Thus, power delivered to the load arrives efficiently while power delivered to the battery arrives inefficiently.

Now take the alternate case where the load current exceeds the input current limit setting. Here the input current limit control engages and the voltage at the intermediate node, V_{OUT}, drops to just under the battery voltage, thus bringing in the battery as a source of additional current. Although this is desired behavior, ensuring load current is prioritized over charge current, notice that there is now inefficiency at the pass element because a large voltage difference does exist between the input pin, again at 5V, and the output pin, which now may be about 3.5V.

From these examples we can see that while a linear PowerPath topology performs the necessary PowerPath control functions under all conditions, it has some inherent inefficiencies. Specifically, with the linear PowerPath topology there is likely to be power wasted in one or the other of the two linear pass elements under various conditions. In the next section we'll see how a switching PowerPath avoids the pitfalls of the linear PowerPath.

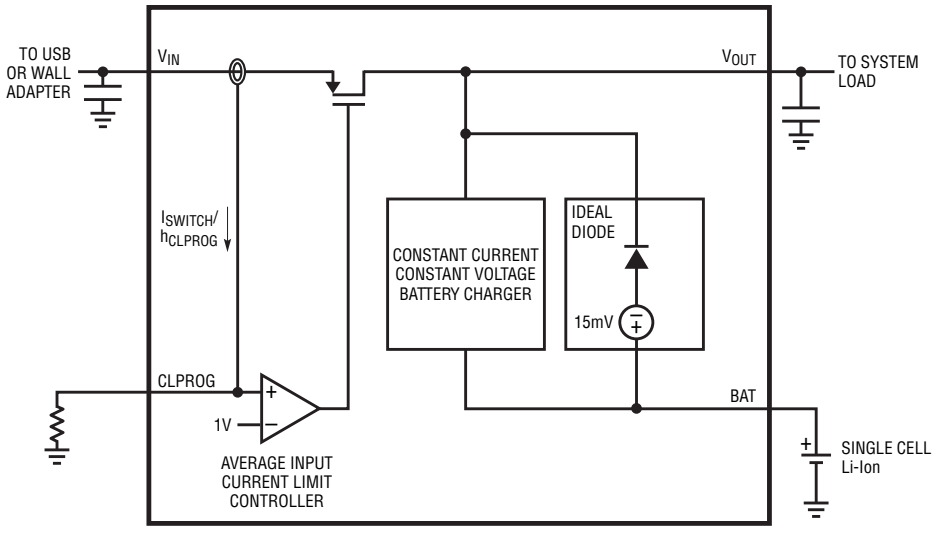


Figure 2. Block diagram of a traditional linear PowerPath, which has significant inherent efficiency limitations.

New School: High Efficiency with Switching PowerPath

Figure 3 shows an alternative to the linear PowerPath, a *switching* PowerPath. Here a step-down DC/DC converter delivers power from the input connector to the intermediate node V_{OUT}. A linear battery charger is connected from the intermediate node to the battery as in the case of the linear PowerPath. The big difference from linear PowerPath is that the path from V_{IN} to V_{OUT} maintains relatively high efficiency regardless of the voltage difference since it is a switching, rather than a linear, path.

Then what about the linear battery charging path, the other big part of

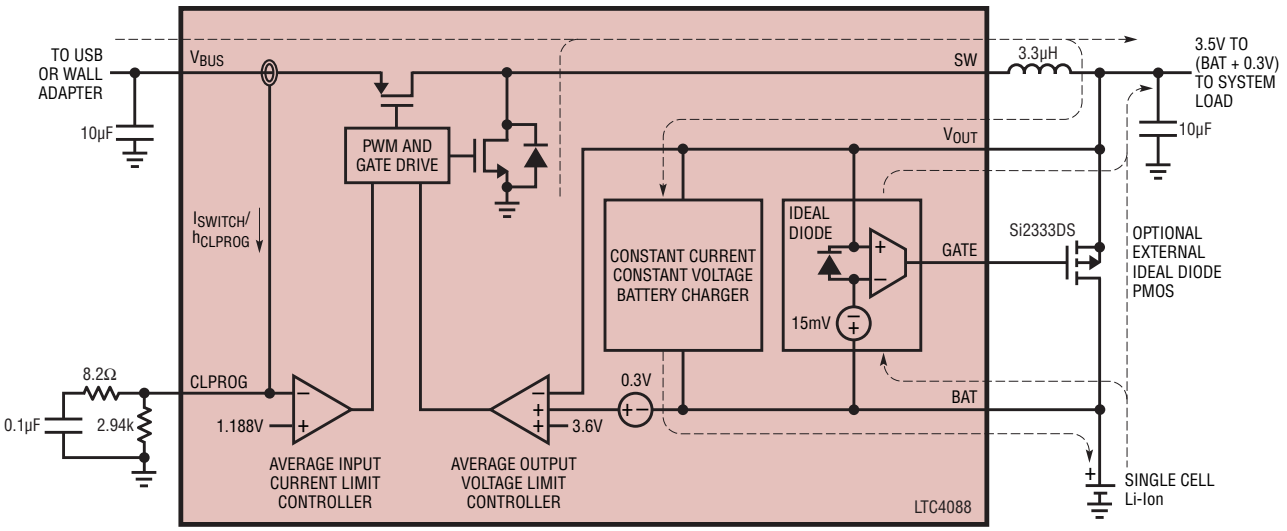


Figure 3. Switching PowerPath block diagram. The big advantage of a switching PowerPath scheme over a linear PowerPath is that the path from V_{IN} to V_{OUT} maintains relatively high efficiency regardless of the V_{IN}/V_{BAT} ratio.

the total efficiency picture? Voltage drops between V_{OUT} and the battery would pretty much erase the efficiency gains made by the switching regulator. Total efficiency remains high with the the LTC4088 and LTC4098 because of a feature called Bat-Track™. With Bat-Track, the output voltage of the switching regulator is programmed to track the battery voltage plus a few hundred millivolt difference. Since the output voltage is never significantly above the battery voltage, little power is ever lost to the linear battery charger. The battery charger pass element leaves most of the voltage control duties to the switching regulator and exists merely to control charge current, float voltage and battery safety monitoring—tasks at which it excels.

USB-Based Constant-Power Charging

These days, an important feature in many portable products is the convenience of charging from a USB port. The LTC4088 and LTC4098 have a unique control system that allows them to limit their input current consumption for USB compliant applications while maximizing power available to the load and battery charging. These two devices not only have low and high power USB settings of 100mA and 500mA, but they also support a higher power 1A setting for wall adapter applications.

For products with large batteries, USB current control can be the limiting factor in determining how much power is delivered to the battery for charging. With a linear PowerPath topology, input and output are current limited—the sum of the load current and the battery charging current cannot exceed the input current. In this case, a switching PowerPath has a significant advantage over a linear PowerPath. In a switching PowerPath topology the input is still current limited, but this only limits available *power* to the load and charger. This is an important distinction. Figure 4 shows an example of how the LTC4088 can provide up to a 40% increase in charge current over a linear PowerPath design.

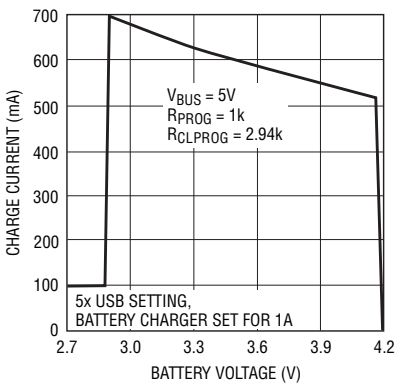


Figure 4. Input power limited charge current

Notice that while the USB current is limited to 500mA, it's possible for the charge current to be above 500mA due to the high efficiency of the switching PowerPath system. So not only does the higher efficiency produce little heat, but it also reduces charge time.

The input current limited topology of the LTC4088 and LTC4098 offers a big advantage over devices that use an output current controlled topology to maintain USB compliance. This is because as the battery voltage rises throughout the charge cycle, the effective power consumed by the battery also rises, assuming a constant current. In order to retain USB compliance in an output current controlled system (assuming perfect efficiency) one would have to limit the battery charge current to its power-limited value at the highest battery voltage.

For example, to remain below 2.5W ($5V_{IN}$ • 500mA) of power delivery at a 4.2V battery voltage, the charge current must not exceed 595mA. This current limit is overly conservative when the battery voltage is low, say 3.4V, where it would be possible to deliver 735mA without violating the USB specification. Input current limited devices designed specifically for USB compliance, such as the LTC4088

and LTC4098, allow the charger to use this additional available current. In contrast, an output current regulated switching charger designed for USB compliance must be programmed to limit battery charging current to the high voltage case (595mA), thus hamstringing it at low battery voltages. Said another way, an input current limited switching charger *always* extracts as much power from the input source as is allowed, whereas an output current controlled one does not.

Instant-On (Low Battery System Start)

Figure 5 shows the instant-on feature of the switching PowerPath topology. When the battery voltage is very low and the system load does not exceed the available programmed power, the output voltage is maintained at approximately 3.6V. This prevents the system from having to wait for the battery voltage to come up before turning on the device—a frustrating scenario to the end user.

This is the primary reason for having a decoupled output node and battery node (i.e. the 3-terminal topology). This feature can be used to power the system in a low power mode. For example, it may be just enough power to start up and indicate to the user that the system is charging.

Automatic Load Prioritization

The current delivered to the system at V_{OUT}, as well as the battery charge current, form a combined load on the switching regulator. If this combined load does not exceed the power level programmed by the input current limit circuit then the switching PowerPath topology happily delivers charge and load current without concern. If, however, the total load exceeds the available power, the battery charger automatically gives up some or all of its share of the power to support the extra load. That is, the system load is always prioritized and battery charging is only performed opportunistically. This algorithm provides uninterrupted power to the system load. Even if the system load alone exceeds the power available from the input limiting circuit, the input current does not exceed its programmed limit. Rather the battery charger shuts off completely and the extra power is drawn from the battery via the ideal diode.

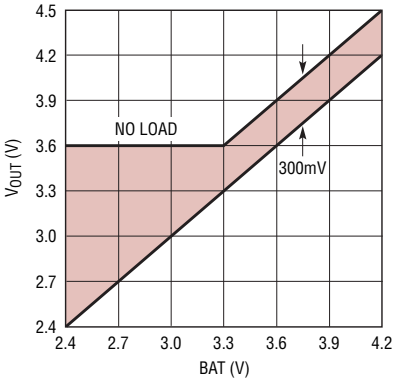


Figure 5. V_{OUT} vs BAT

When the ideal diode is engaged, the conduction path from the battery to the output pin is approximately 180mΩ. If this is sufficient for the application, then no external components are needed. If greater conductance is necessary, however, an external MOSFET can be used to supplement the internal ideal diode. The LTC4088 and LTC4098 both have a control pin for driving the gate of the optional external transistor. Transistors with resistance of 30mΩ or lower can be used to supplement the internal ideal diode.

Full Featured Battery Charger

The LTC4088 and LTC4098 both include a full featured battery charger. The battery chargers feature programmable charge current, cell preconditioning with bad-cell detection and termination, CC-CV charging, C/10 end of charge detection, safety timer termination, automatic recharge and a thermistor signal conditioner for temperature qualified charging.

LTC4098 Enhancements

The LTC4098 has a few features that the LTC4088 does not. First, it supports the ability to control an external high voltage switching regulator to receive power from a second input supply such an automobile battery. It also includes an independent overvoltage protection module that can, in conjunction with an external MOSFET, provide significant input protection to the low voltage (USB/WALL) input.

High Voltage Input Controller

The LTC4098's external input control circuit recognizes when a second input supply is present and prioritizes that input in the event that both it and the USB/WALL input are powered simultaneously. Furthermore, the LTC4098 interfaces with a number of Linear Technology high voltage step-down switching regulators to allow for higher voltage inputs, such as an automotive battery. Using the same Bat-Track technique described above, the auxiliary input controller commands the high voltage regulator to develop a voltage at V_{OUT} that tracks just above the battery. Again, this technique results in high charging efficiency even when charging from a fairly high voltage.

Overvoltage Protection

The LTC4098 includes an overvoltage protection controller that can be used to protect the low voltage USB/Wall input from the inadvertent application of high voltage or from a failed wall adapter. This circuit controls the gate of an external high voltage N-type MOSFET. By using an external transistor for high voltage standoff, the protection level is not limited to the process parameters of the LTC4098. Rather the specifications of the external transistor determine the level of protection provided.

Conclusion

The LTC4088 and LTC4098 represent a new paradigm in power management and battery charging. Both optimize power delivery by combining constant input power limiting with a high efficiency switching regulator and Bat-Track battery charging. Other benefits include instant-on system starting, automatic load prioritization and unmatched charging efficiency. The LTC4098 goes a step beyond with an auxiliary input controller for higher input voltages (such as a car battery) and an overvoltage protection controller.

Hot Swap Controller Enables Standard Power Supplies to Share Load

by Vladimir Ostrerov

Introduction

The LTC4350 Hot Swap™ and load share controller is a powerful tool for developing high availability redundant and load sharing power supply systems. It has the unique ability to work with supplies with any output stage topology, including output stages using synchronous rectification.

Although the LTC4350 does much of the heavy lifting in maintaining a well balanced load share system, there are a number of important considerations in designing a stable system.

This article deals with some of the more complex design details of the LTC4350. If you are designing a load share system and LTC4350 is new to you, it may be helpful to first read introductory details in the LTC4350 data sheet, and the article "Combo/Hot Swap Load Share Controller Allows the use of Standard Power Modules in Redundant Power Systems" in the June, 2003 issue of *Linear Technology* magazine.

A Little Background

DC/DC converters are paralleled for any of several reasons:

- **One converter may be insufficient for the required power level.** For example, an existing single regulator design may be able to handle 100W, but a new application calls for up to 200W. Paralleling two, production-proven 100W converters saves time over developing a new converter capable of twice the power.
- **The product may need to be scalable.** Many rack-based systems feature multiple slots, which may be populated at some future date, but why install power supply sufficient to operate the entire rack when only a fraction of the slots are in use? Paralleling supplies allows addition of power on an as-needed basis.
- **Redundancy.** These systems, often called N + 1 redundant, use a number of small supplies where N units are needed to power the load, but a "+1" supply is added for redundancy. The theory is, if one supply fails, N units remain to carry the load.
- **Efficiency.** If the power system must support widely ranging loads, efficiency can be optimized by adjusting the number of operating supplies to the load.

The LTC4350 Hot Swap and load share controller is a powerful tool for developing high availability redundant and load sharing power supply systems.

It has the unique ability to work with supplies with any output stage topology, including output stages using synchronous rectification.

The key to parallel operation is balancing the output current of each supply, so that all are equally loaded if the supplies are identical. If individual supplies with different power ratings are combined for parallel operation, the output current of each supply must be proportional to the rated supply power.

The LTC4350 performs this function. It forces multiple, paralleled power supplies to share current. The concept behind a LTC4350-based load share controller is simple: a single, overall voltage loop controls the common output while each power converter is controlled by a local current loop and contributes current in the common output. Even so, such a multi-loop feedback system requires careful design.

Active control is achieved by sinking additional current from the +SENSE pin found on many common converter modules, and fooling the converter into believing the output voltage is something different than what it would otherwise detect. Increasing this current causes the output to rise; decreasing it causes the output to fall. Thus the LTC4350 has a means of modulating the output voltage, thereby controlling the companion converter's contribution to the system.

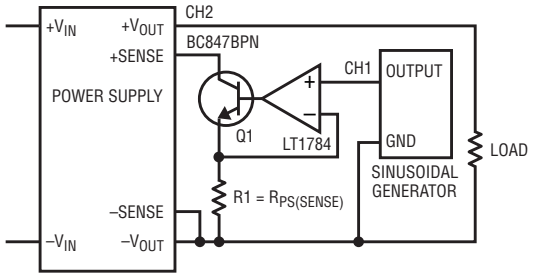


Figure 1. Power supply closed-loop Bode plot measurement block diagram

AC Analysis

The design of a current sharing power system involves not only the simple matter of DC operating conditions, but also AC analysis. This article covers the AC design aspects of an LTC4350-based load share system.

The design goal is to build a stable system with maximum bandwidth,

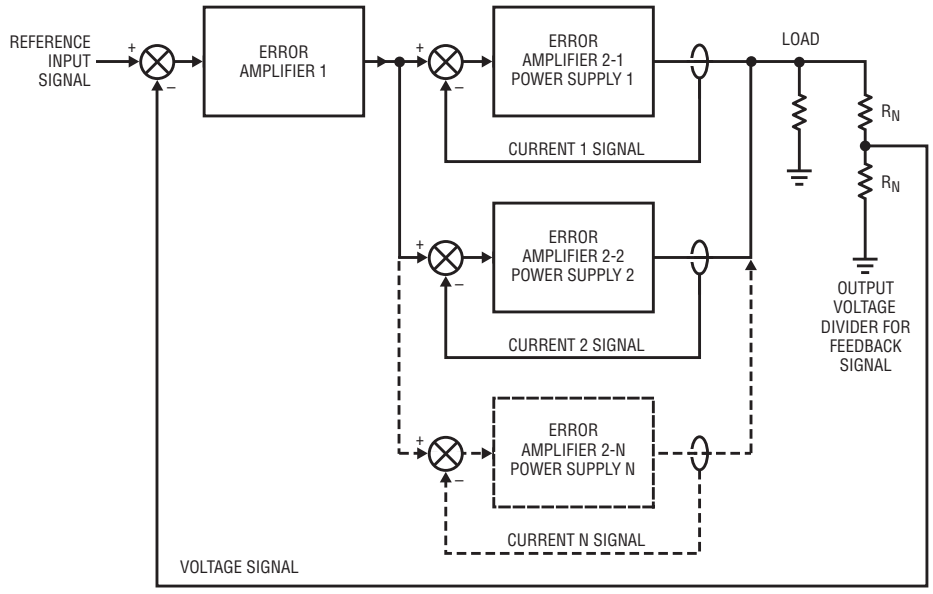


Figure 2. Power system control loop

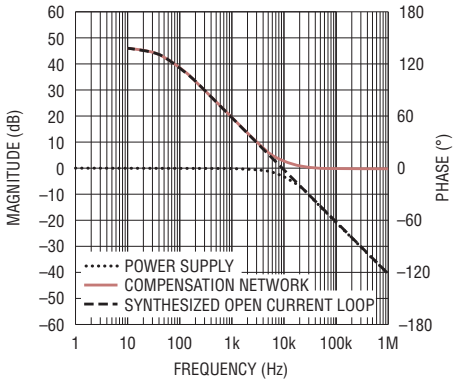


Figure 3. Current loop Bode design with power supply having first order transfer function

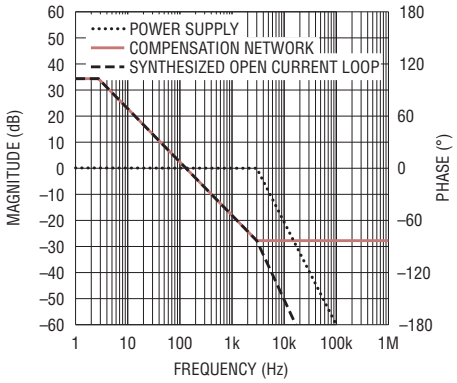


Figure 4. Current loop synthesis with 0,–1,–2 shape

with good transient response, and to preserve as much of the inherent performance of the individual power supply as possible.

As each supply in a power system is a fixed configuration component, knowledge of its main characteristics is indispensable for control system design. Among the power supply characteristics essential for design purposes are power supply bandwidth, output stage topology and power supply output voltage ramp up behavior.

Figures for power supply bandwidth can be obtained directly from the power supply manufacturer or measured in the lab. One way to experimentally measure bandwidth is to use a simple driver, a sine wave generator and an oscilloscope. Figure 1 shows the block diagram for this measurement. Scope probes are connected to the generator output and power supply output. A power supply Bode plot can be obtained significantly faster using special equipment for frequency response measurement, such as a VENABLE Frequency Response Analyzer or AP's Analog Network Analyzer. Power supply bandwidth should be measured with 90%–100% load.

The power supply output stage topology should be taken into account when designing the load share power system. If it is a synchronously rectified power supply output stage, it is able to provide bidirectional energy flow and as a result the power supply can operate in the second quadrant and sink current. In this case one of two special measures should be taken: either synchronize the activation of the LTC4350 controller current share ability with the MOSFET switch turn-on process, or disable synchronous rectification before the LTC4350 load share capability is activated. Detailed descriptions of those actions are presented below.

The power supply output voltage ramp-up behavior during turn on should be checked to eliminate LTC4350 operation in the area where output voltage slew rate experiences significant changes. An undervoltage protection circuit, which is connected with pin 1, performs this function.

Unified Approach to Compensation Components Parameters Evaluation

A power system with K power supplies operating in parallel is a K + 1 loop control system. This system has one voltage loop, which is the highest bandwidth loop, and K current loops. These K current loops work with a common input command signal and individual feedback current signals. All current loops operate in parallel. A block diagram of the control loops is shown in Figure 2.

There are two restrictions on loop bandwidth. All current loops must have equal bandwidths. The voltage loop bandwidth must be wider than any current loop bandwidth to eliminate current oscillation between power supplies.

LTC4350 error amplifiers EA1 and EA2 are transconductance operational amplifiers. This restricts compensation circuit transfer functions to two types: pole or a pole and zero with $T_{POLE} > T_{ZERO}$. A compensation circuit of one capacitor C_C implements a transfer function

$$\frac{G_{EA}}{T_{POLE}s+1} \qquad [1]$$

where G_{EA} is the error amplifier voltage gain, g_mR_O, and,

$$T_{POLE} = \frac{1}{2\pi R_O C_C}.$$

R_O is the internal error amplifier's output impedance.

If a compensation circuit has capacitor C_C and resistor R_C series connected, it implements a transfer function

$$\frac{G_{EA}(T_{ZERO}s+1)}{T_{POLE}s+1} \quad [2]$$

where

$$T_{ZERO}=\frac{1}{2\pi R_C C_C}$$

The equations shown are based on the assumption that $R_O >> R_C$.

Current Control Loop Synthesis and Compensation Component Calculation

The Bode amplitude characteristic slope is defined by the integer K (0, 1, 2, etc.) to express the slope

$$SLOPE=(-20\frac{db}{dec}\bullet K)$$

As an outer loop, the voltage loop must have larger bandwidth than the inner current loop. The closed current loop Bode plot should be shaped as 0,–1 or 0,–1,–2 with the –1 segment at least 1.4 decades long.

1. If the power supply Bode amplitude characteristic has shape 0,–1 or 0,–1,–2, and the –1 segment is 1.4 decades long, the current loop error amplifier compensation network allows for a current loop bandwidth equal to the power supply bandwidth. This can be achieved by tailoring the current loop compensation network so that its zero frequency is equal to the main power supply pole frequency. Figure 3 demonstrates this approach.
2. If the power supply Bode amplitude characteristic has shape 0,–1,–2, and the –1 segment is shorter than 1.4 decades—or at the extreme, the shape is 0,–2—shifting the current loop crossover frequency to the left (this reduces the current loop bandwidth to below the power supply bandwidth) makes it possible to achieve a 0,–1,–2 closed current loop shape with the –1 segment covering least 1.4 decades. In the extreme case when the power supply closed loop frequency response characteristic is 0,–2, placing a compensation network zero exactly at the coordinate where the amplitude is –28db and the frequency is the power supply bandwidth, and placing the pole value so that the crossover frequency is 25× lower than the power supply bandwidth achieves the desired result. Figure 4 illustrates synthesis of a current loop with shape 0,–1,–2.

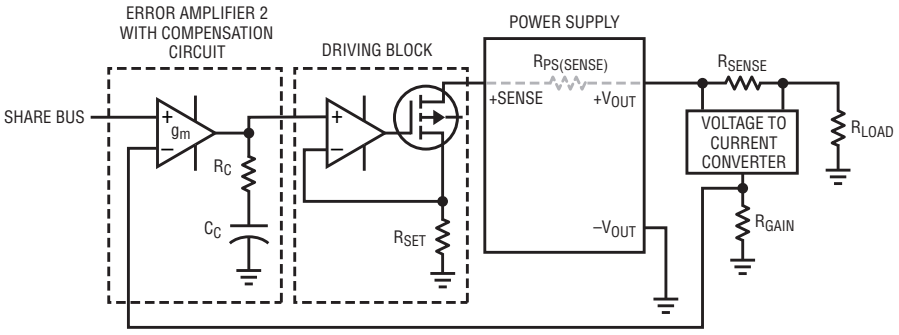


Figure 5. Current loop functional block diagram

A current loop block diagram and current loop control diagram are shown in Figures 5 and 6.

Current open-loop gain is proportional to load and it must be calculated at the power supply's maximum available current. At maximum load current (I_{LIMIT}), an additional 1V output on the power supply produces additional current in the load as given by

$$\Delta I=\frac{I_{LIMIT}}{V_{OUT}}$$

and produces a corresponding signal on the sense resistor as follows

$$\Delta V_{SENSE}=\frac{I_{LIMIT}R_{SENSE}}{V_{OUT}}.$$

Current open-loop gain equals

$$G_{CO}=G_{EA2}\bullet G_{DB}\bullet G_{CSA},$$

where G_{EA2} is the error amplifier EA2 gain, G_{DB} is the driving block gain, and G_{CSA} is the current sense amplifier gain, which is given by

$$G_{CSA}=\frac{I_{LIMIT}R_{SENSE}}{V_{OUT}}\bullet 10^{-3}\bullet R_{GAIN}$$

It should be noted that R_{SENSE} is a resistor connecting the power sup-

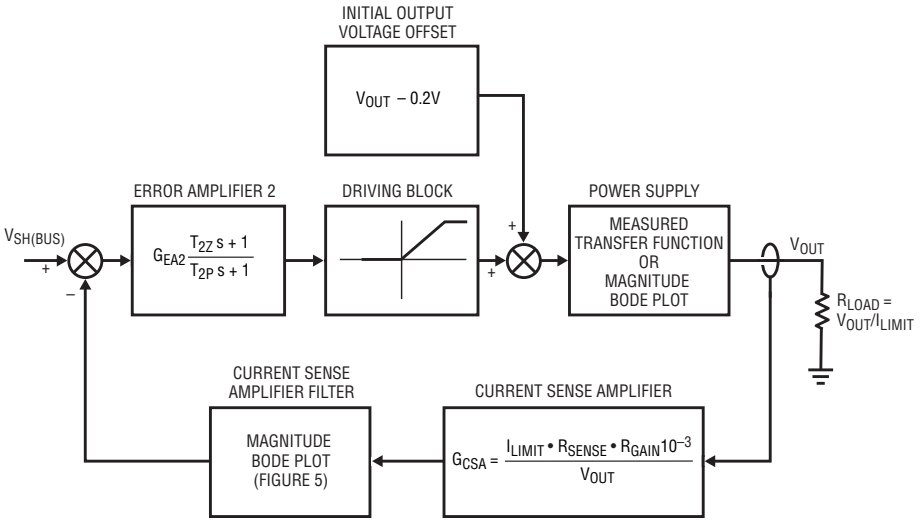


Figure 6. Current loop control block diagram

ply output to the load. Driving block gain is

$$G_{DB} = \frac{R_{PS(SENSE)}}{R_{SET}}$$

where $R_{PS(SENSE)}$ is a power supply resistor value and R_{SET} is a resistor connected to the LTC4350 SET pin.

The LTC4350's voltage-to-current converter in the current sensing block has a flat response from low frequencies up to 10kHz, where a low frequency pass filter is implemented.

Measured Error Amplifier 2 voltage gain is 500–1000.

Voltage Control Loop Synthesis and Compensation Component Calculation

The voltage loop forward path contains an error amplifier (Error Amplifier 1) and the current loop, and the feedback path contains an output voltage divider. A control diagram for the voltage loop is shown in Figure 7.

Measured Error Amplifier 1 voltage gain is 1800–2200.

Bode design for the voltage loop is demonstrated in Figures 8 and 9. The first plot explains the design when the current closed-loop magnitude response has shape 0,–1. To have a voltage loop crossover frequency 6 to 7 times wider than the current closed-loop bandwidth, the compensation should have a zero at the same frequency as the bandwidth, but the magnitude of the gain must be 15dB – 17dB [20log(6) = 15.5; 20log(7) = 16.9]. The pole frequency equals

$$f_{1(POLE)} = (3-6)\frac{f_{1(ZERO)}}{G_{V(OPEN)}}$$

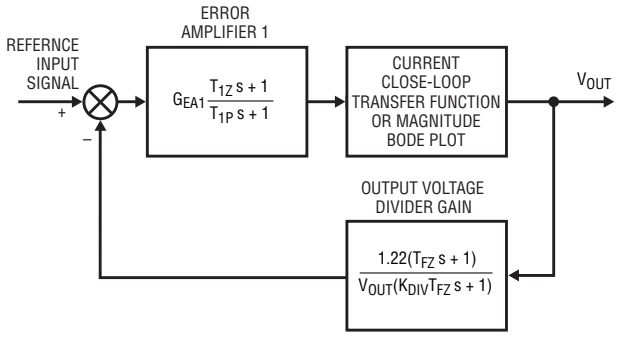


Figure 7. Voltage loop control block diagram

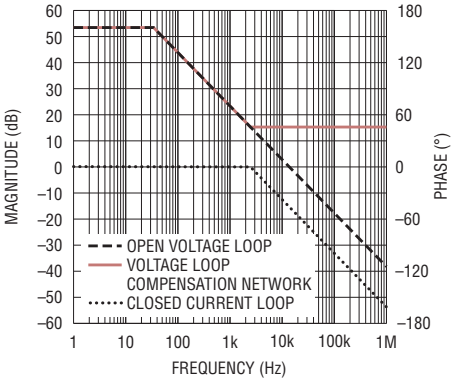


Figure 8. Voltage loop Bode design with current closed loop having 0,–1 shape

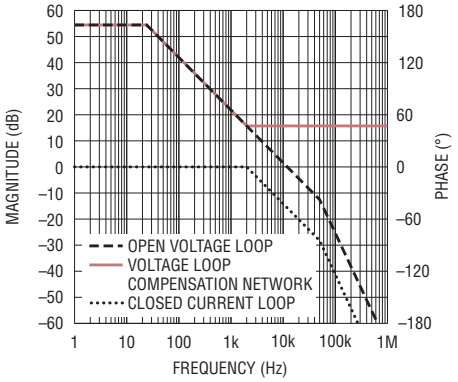


Figure 9. Voltage loop Bode design with closed current loop having 0,–1,–2 shape

where $G_{V(OPEN)}$ is the voltage open-loop gain.

The same relationship between voltage loop crossover frequency and the current closed-loop bandwidth should hold in the second case, when the current closed-loop magnitude response is shaped as 0,–1,–2. The compensation provided should be the same as the first case, as shown in Figure 9.

An additional option exists for improvement of the voltage open-loop magnitude response by placing in the feedback path lead compensation with lead ratio $1.22/V_{OUT}$. Shunting the top resistor in the output voltage divider with a capacitor implements the transfer function

$$\frac{T_{f(ZERO)}s+1}{T_{f(POLE)}s+1}\bullet\frac{1.22}{V_{OUT}}$$

where

$$T_{f(ZERO)} = R_{f1}C_f$$

and

$$T_{f(POLE)} = T_{f(ZERO)}\bullet\frac{V_{OUT}}{1.22}$$

R_{f1} is the top resistor in the voltage divider and C_f is the shunting capacitor. This compensation allows bending of the magnitude response and gives a slope of –20db/dec around the crossover frequency in the restricted frequency area. It is the maximum area for a 12V system; it takes

$$20\log\frac{12}{1.22} = 19.85db$$

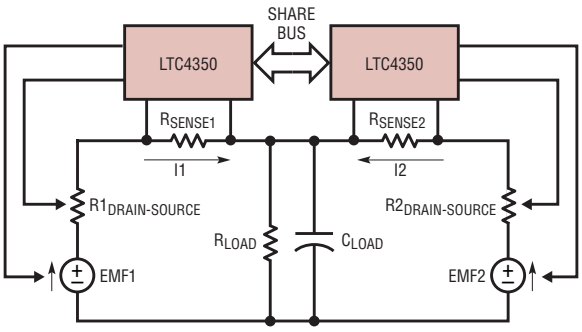


Figure 10. Output power stage equivalent circuitry. The power supply output characteristic exists in the second quadrant

continued on page 16

Understanding IP2 and IP3 Issues in Direct Conversion Receivers for WCDMA Wide Area Basestations

by Doug Stuetzle

Introduction

A direct conversion receiver architecture offers several advantages over the traditional superheterodyne. It eases the requirements for RF front end bandpass filtering, as it is not susceptible to signals at the image frequency. The RF bandpass filters need only attenuate strong out-of-band signals to prevent them from overloading the front end. Also, direct conversion eliminates the need for IF amplifiers and bandpass filters. Instead, the RF input signal is directly converted to baseband, where amplification and filtering are much less difficult. The overall complexity and parts count of the receiver are reduced as well.

Direct conversion does, however, come with its own set of implementation issues. Since the receive LO signal is at the same frequency as the RF signal, it can easily radiate from the receive antenna and violate regulatory standards. Also, a thorough understanding of the impact of the IP2 and IP3 issues is required. These parameters are critical to the overall performance of the receiver and the key component is the I/Q demodulator.

Unwanted baseband signals can be generated by 2nd order nonlinearity of the receiver. A tone at any frequency entering the receiver gives rise to a DC offset in the baseband circuits. Once generated, straightforward elimination of DC offset becomes very problematic. That is because the frequency response of the post-downconversion circuits must often extend to DC. The 2nd order nonlinearity of the receiver also allows a modulated signal—even the desired signal—to generate a pseudo-random block of energy centered about DC.

Unlike superheterodyne receivers, direct conversion receivers are susceptible to such 2nd order mechanisms regardless of the frequency of the incoming signal. So minimizing the effect of finite 2nd order linearity is critical.

Later in this article we consider the effect of 3rd order distortion on a direct conversion receiver. In this case, two signals separated by an appropriate frequency must enter the receiver in order for unwanted products to appear at the baseband frequencies.

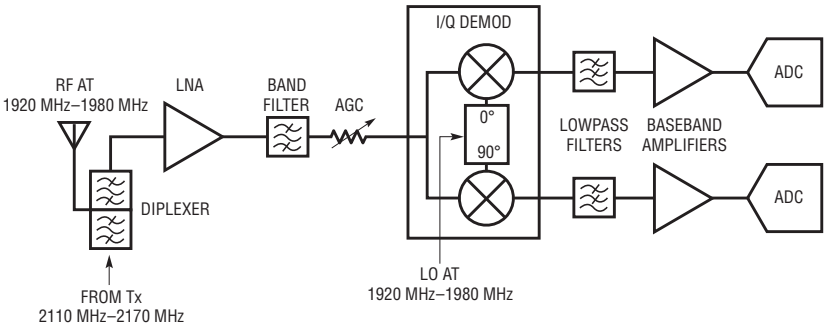


Figure 1. Direct conversion receiver architecture

Second Order Distortion (IP2)

The second order intercept point (IP2) of a direct conversion receiver system is a critical performance parameter. It is a measure of second order non-linearity and helps quantify the receiver's susceptibility to single- and 2-tone interfering signals. Let's examine how this nonlinearity affects sensitivity.

We can model the transfer function of any nonlinear element as a Taylor series:

$$y(t) = x(t) + a_2x^2(t) + a_3x^3(t) + \ldots$$

where x(t) is the input signal consisting of both desired and undesired signals. Consider only the second order distortion term for this analysis. The coefficient a_2 is equal to

$$a_2 = \sqrt{\frac{2}{Z_0 IP2}}$$

where IP2 is the single tone intercept point in watts. Note that the 2-tone IP2 is 6dB below the single-tone IP2. The more linear the element, the smaller a_2 is.

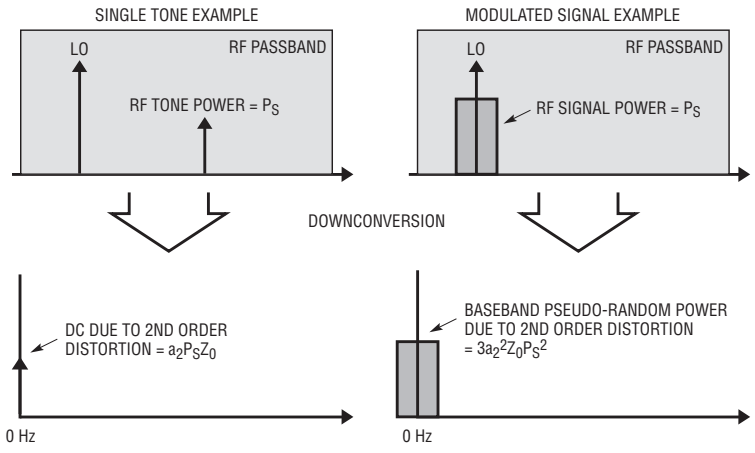


Figure 2. Effects of 2nd order distortion

Every signal entering the nonlinear element generates a signal centered at zero frequency. Even the desired signal gives rise to distortion products at baseband. To illustrate this, let the input signal be represented by x(t) = A(t)cosωt, which may be a tone or a modulated signal. If it is a tone, then A(t) is simply a constant. If it is a modulated signal, then A(t) represents the signal envelope.

By definition, the power of the desired signal is

$$P_S = \frac{1}{Z_0} \bullet E\left\{\left[A(t)\cos\omega t\right]^2\right\}$$

where E{β} is the expected value of β. Since A(t) and cosωt are statistically independent, we can expand $E\{(A(t)\cos\omega t)^2\}$ as $E\{A^2(t)\} \bullet E\{\cos^2\omega t\}$. By trigonometry

$$P_S = \frac{1}{Z_0} \bullet E\left\{A^2(t)\right\} \bullet E\left\{\frac{1+\cos 2\omega t}{2}\right\}$$

The expected value of the second term is simply ½, so the power of the desired signal simplifies to:

$$P_S = \frac{1}{2Z_0} \bullet E\left\{A^2(t)\right\} \quad [1]$$

In the case of a tone, A(t) may be replaced by A. The signal power is, as expected, equal to

$$P_S = \frac{A^2}{2Z_0}$$

In the more general case, the desired signal is digitally modulated by a pseudo-random data source. We can represent it as bandlimited white noise with a Gaussian probability distribution. The signal envelope A(t) is now a Gaussian random variable. The expected value of the square of the envelope can be expressed in terms of the power of the desired signal as:

$$E\left\{A^2(t)\right\} = 2Z_0P_S \quad [2]$$

Now substitute x(t) into the Taylor series expansion to find y(t), which is the output of the nonlinear element:

$$y(t) = A(t)\cos\omega t + a_2\left[A(t)\cos\omega t\right]^2 + \ldots \text{Higher Order Terms}$$

$$= A(t)\cos\omega t + \frac{1}{2}a_2A^2(t) + \frac{1}{2}a_2A^2(t)\cos 2\omega t \ldots$$

Consider the 2nd order distortion term $\frac{1}{2}a_2[A(t)]^2$. This term appears centered about DC, whereas the other 2nd order term appears near the 2nd harmonic of the desired signal. Only the term near DC is important here, as the high frequency tone is rejected by the baseband circuitry.

In the case where the signal is a tone, the 2nd order result is a DC offset equal to:

$$\text{DC OFFSET} = \frac{1}{2} \bullet a_2A^2 = a_2P_SZ_0 \quad [3]$$

If the desired signal is modulated, then the 2nd order result is a modulated baseband signal. The power of this term is

$$P_{BB} = \frac{1}{Z_0} \bullet E\left\{\left[\frac{1}{2}a_2A^2(t)\right]^2\right\}$$

This can be expanded to:

$$P_{BB} = \frac{(a_2)^2}{4Z_0} \bullet E\left\{A^4(t)\right\} \quad [4]$$

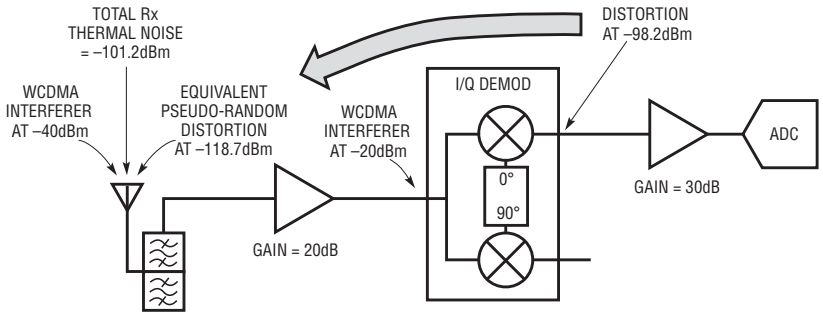


Figure 3. 2nd Order distortion due to WCDMA carrier

In order to express this result in terms of the desired signal power, we must relate $E\{A^4(t)\}$ to $E\{A^2(t)\}$. For a Gaussian random variable, the following relation is true:

$$E\left\{A^4(t)\right\} = 3 \bullet \left[E\left\{A^2(t)\right\}\right]^2 \quad [5]$$

The distortion power can then be expressed as

$$P_{BB} = \frac{3(a_2)^2}{4Z_0} \bullet \left[E\left\{A^2(t)\right\}\right]^2$$

Now express the expected value in terms of the desired signal power:

$$P_{BB} = 3(a_2)^2 Z_0 (P_S)^2 \quad [6]$$

It is the conversion of any given tone to DC, and any modulated signal into a baseband signal that makes 2nd order performance critical to direct conversion receiver performance. Unlike other nonlinear mechanisms, the signal frequency does not determine where the distortion product falls.

Any two signals entering the nonlinear element give rise to a beat note/term. Let

$x(t) = A(t)\cos\omega t + B(t)\cos\omega_u t,$

where the first term is the desired signal and the second term is an unwanted signal.

$$y(t) = A(t)\cos\omega t + a_2\left[A(t)\cos\omega t + B(t)\cos\omega_u t\right]^2 + \ldots \text{Higher Order Terms}$$

$$= A(t)\cos\omega t + \frac{1}{2}a_2A^2(t) + \frac{1}{2}a_2A^2(t)\cos 2\omega t + 2a_2A(t)B(t)\cos\omega t\cos\omega_u t \ldots$$

$$= A(t)\cos\omega t + \ldots + a_2A(t)B(t)\cos(\omega - \omega_u)t \ldots$$

The second order distortion term of interest is $a_2A(t)B(t)\cos(\omega - \omega_u)t$. This term describes the distortion product centered about the difference frequency between the two input signals. In the case of two unwanted tones entering the element, the result includes a tone at the difference frequency. If the two

unwanted signals are modulated, then the resultant includes a modulated signal centered about their difference frequency.

We can apply these principles to a direct conversion receiver example. Figure 1 shows the block diagram of a typical WCDMA basestation receiver. Here are some key characteristics of this example:

- ❑ Basestation Type: FDD, Band I
- ❑ Basestation Class: Wide Area
- ❑ Number of carriers: 1
- ❑ Receive band: 1920MHz to 1980MHz
- ❑ Transmit band: 2110MHz to 2170MHz

The RF section of this receiver includes a diplexer, a bandpass filter, and at least one Low Noise Amplifier (LNA). The frequency selective elements are used to attenuate out-of-band signals and noise. The LNA(s) establishes the noise figure of the receiver. The I/Q demodulator converts the receive signal to baseband.

In the examples illustrated below, the characteristics of the LT5575 I/Q demodulator as representative of a basestation class device of this type. Lowpass filters and baseband amplifiers bandlimit and increase the signal level before it is passed to the A/D converters. The diplexer and RF bandpass filter serve as band filters only; they do not offer any carrier selectivity.

The second order linearity of the LNA is much less important than that of the demodulator. This is because any LNA distortion due to a single signal is be centered about DC and rejected by the demodulator. If there are two unwanted signals in the receive band (1960MHz, for example), then a second order product is generated by the LNA at the difference frequency. This signal is demodulated and appears as a baseband artifact at the A/D converter. We need not address this condition, however, because out of band signals emerging from the front end diplexer are not strong enough to create distortion products of any importance.

Consider first a single unmodulated tone entering the receiver (see Figure 2). As detailed above, this tone gives rise to a DC offset at the output of the demodulator. If the baseband cascade following the demodulator is DC-coupled, this offset is applied to the A/D converter, reducing its dynamic range. The WCDMA specification (3GPP TS 25104.740) calls out an out-of-band tone at –15dBm, located 20MHz or more from either receive band edge (section 7.5.1). Compute the DC offset generated in the I/Q demodulator:

- ❑ Tone entering receive antenna port: –15dBm
- ❑ Diplexer rejection at 20MHz offset: 0dB
- ❑ Bandpass rejection at 20MHz offset: 2dB
- ❑ RF gain preceding LT5575: 20dB
- ❑ Tone entering LT5575: 3dBm
- ❑ LT5575 IIP2, 2-tone: 60dBm
- ❑ LT5575 a_2: 0.00317
- ❑ DC offset at LT5575 output: 0.32mV
- ❑ Baseband voltage gain: 31.6
- ❑ DC offset at A/D input: 10mV

Single WCDMA carriers can also serve as interferers, as detailed in section 7.5.1. In one case, this carrier is offset by at least 10MHz from the desired carrier, but is still in the receive band. The power level is –40dBm, and the receiver must meet a sensitivity of –115dBm for a 12.2kbps signal at a BER of 0.1%. Here are the details:

- ❑ Signal entering receive antenna port: –40dBm
- ❑ RF gain preceding LT5575: 20dB
- ❑ Signal entering LT5575: –20dBm
- ❑ LT5575 IIP2, 2-tone: 60dBm
- ❑ LT5575 a_2: 0.00317

A MATLAB simulation performed using a pseudo-random channel predicts a distortion at the LT5575 output of –98.7dBm. This result agrees well with that given by equation 6, which predicts a distortion power of –98.2dBm.

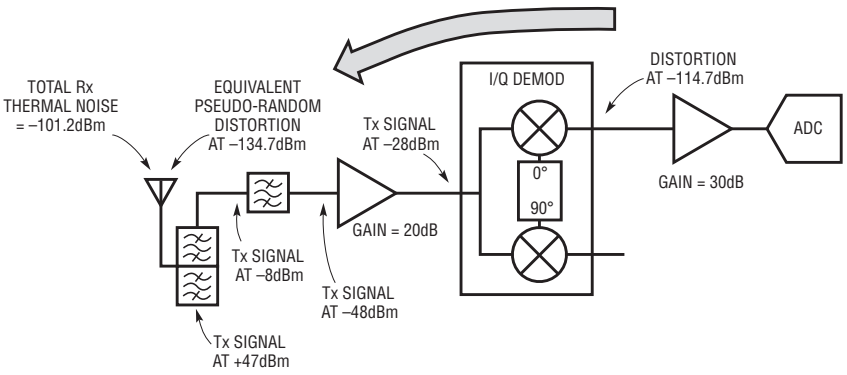


Figure 4. Transmitter leakage effects

The baseband product that appears at the LT5575 output is a noiselike signal, created from the interfering WCDMA carrier. If this signal is large enough, it can add to the thermal receiver and A/D converter noise to degrade sensitivity. Compute the equivalent thermal noise at the receiver input with no added distortion:

- ❑ Sensitivity: –121dBm
- ❑ Processing + coding gain: 25dB
- ❑ Signal to noise ratio at sensitivity: 5.2dB
- ❑ Thermal noise at receiver input: –101.2dBm

Now refer the distortion signal back to the receiver input:

- ❑ RF gain preceding LT5575: 20dB
- ❑ Equivalent interference level at Rx input: –118.7dBm

The baseband second order product in this case is 17.5dB below the thermal noise at the receiver input. The resulting degradation in sensitivity is <0.1dB, so the receiver easily meets the specification of –115dBm. This is illustrated in Figure 3. Single WCDMA carriers can also appear out of band, as specified in section 7.5.1. These can be directly adjacent to the receive band at levels as high as –40dBm. Here again, the second order effect of such carriers upon sensitivity is negligible, as the preceding analysis shows.

Another threat to sensitivity comes from transmitter leakage in FDD systems, as shown in Figure 4. In an FDD system, the transmitter and receiver

are operating at the same time. For the WCDMA Band I case, the transmit band is 130MHz above the receive band. A single antenna is commonly used, with the transmitter and receiver joined by a diplexer. Here are some typical basestation coupled resonator-type diplexer specifications:

- ❑ Isolation, Tx to Rx 2110MHz: 55dB
- ❑ Diplexer insertion loss, Tx path: 1.2dB

In the case of a Wide Area basestation, the transmit power may be as high as 46dBm. At the transmit port of the diplexer the power is at least 47dBm. This high level modulated signal leaks to the receiver input, and some portion of it drives the I/Q demodulator:

- ❑ Receiver input power: –8dBm
- ❑ Rx BPF rejection at 2110MHz: 40dB
- ❑ RF gain preceding LT5575: 20dB
- ❑ Signal entering LT5575: –28dBm
- ❑ LT5575 IIP2, 2-tone: 60dBm
- ❑ LT5575 a_2: 0.00317

A MATLAB simulation performed using a pseudo-random channel predicts the following:

- ❑ Distortion at LT5575 output: –114.7dBm

Refer this signal back to the receiver input:

- ❑ RF gain preceding LT5575: 20dB
- ❑ Equivalent interference level at Rx input: –134.7dBm
- ❑ Thermal noise at receiver input: –101.2dBm

This equivalent interference is 33.5dB below the thermal noise at the receiver input. The resulting degradation in sensitivity is <0.1dB, so the receiver easily meets the specification of –121dBm.

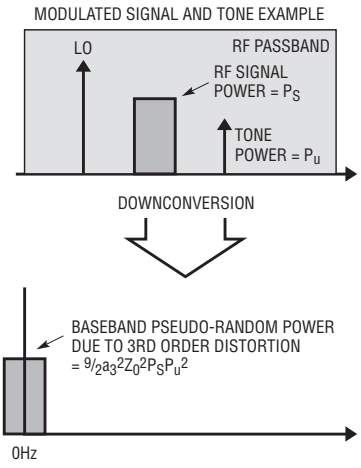


Figure 5. Effects of 3rd order distortion

Third Order Distortion (IP3)

The third order intercept point (IP3) has an effect upon the baseband signal when two properly spaced channels or signals enter the nonlinear element.

Refer back to the transfer function: $y(t) = x(t) + a_2x^2(t) + a_3x^3(t) + \ldots$, where x(t) is the input signal consisting of both desired and undesired signals. Consider now the third order distortion term. The coefficient a_3 is equal to $2/(3Z_0IP3)$ where IP3 is the single tone intercept point in Watts. Note that the 2-tone IP3 is 4.78dB below the single-tone IP3.

Two signals entering the nonlinear element generate a signal centered at zero frequency if the spacing between the two signals is equal to the distance to zero frequency. Let $x(t) = A(t)\cos\omega t + B(t)\cos\omega_u t$, where the first term is the desired signal and the second term is an unwanted signal. The unwanted signal may be a tone or a modulated signal. If it is a tone, then B(t) is simply a constant. If it is a modulated signal, then B(t) represents the signal envelope.

The output signal is then equal to y(t):

$$y(t) = A(t)\cos\omega t + \ldots + a_3\left[A(t)\cos\omega t + B(t)\cos\omega_u t\right]^3 + \ldots \text{Higher Order Terms}$$

$$= A(t)\cos\omega t + \ldots + 3a_3A^2(t)B(t)\cos^2\omega t\cos\omega_u t + 3a_3A(t)B^2(t)\cos\omega t\cos^2\omega_u t \ldots$$

$$= A(t)\cos\omega t + \ldots + \frac{3}{4}a_3A(t)B^2(t)\cos(2\omega_u - \omega)t \ldots$$

The third order distortion term of interest here is $\frac{3}{4}a_3A(t)B^2(t)\cos(2\omega_u - \omega)t$. In order for this distortion to appear at baseband, set $\omega = 2\omega_u$. The power of the distortion is

$$P_{BB} = \frac{1}{Z_0} \bullet E\left\{\left[\frac{3}{4}a_3A(t)B^2(t)\right]^2\right\}$$

which can be expanded to

$$P_{BB} = \frac{9(a_3)^2}{16Z_0} \bullet E\left\{A^2(t)\right\} \bullet E\left\{B^4(t)\right\} \quad [7]$$

Consider the case of a modulated desired signal and a tone interferer; B(t) may be replaced by B. See Figure 5. The value of $E\{B^4\}$ can be expressed as $(2Z_0P_u)^2$, where P_u is the power of the tone interferer. We can use Equation 2 to express $E\{A^2(t)\}$ in terms of the desired signal power as $2Z_oP_s$, where P_s is the power of the desired signal. The power level of the distortion at baseband is then:

$$P_{BB} = \frac{9}{2} \bullet P_S(P_u)^2(Z_0)^2(a_3)^2 \quad [8]$$

If the undesired signal is modulated, use Equations 2 and 5 to express $E\{B^4(t)\}$ as $3(2Z_0P_u)^2$, where P_u is the power of the tone interferer:

$$P_{BB} = \frac{27}{2} \bullet (a_3)^2(Z_0)^2P_S(P_u)^2 \quad [9]$$

In the direct conversion receiver example, Section 7.6.1 of the WCDMA specification calls for two interfering

continued on page 27

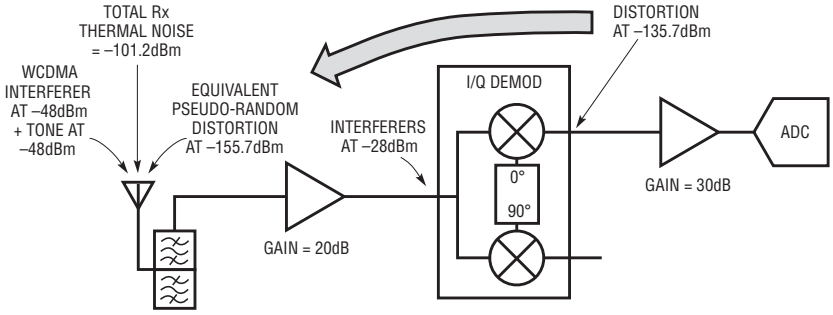


Figure 6. 3rd Order distortion due to WCDMA carrier + tone interferer

Complete Dual-Channel Receiver Combines 14-Bit, 125Msps ADCs, Fixed-Gain Amplifiers and Antialias Filters in a Single 11.25mm × 15mm µModule Package

by Todd Nelson

Introduction

Extensive hands-on applications experience is a prerequisite for any designer hoping to take full advantage of an ADC's capabilities when sampling high dynamic range signals in multichannel IF-sampling or in I/Q baseband communications channels. An intimate knowledge of the amplifier output stage and ADC front end is required to match the impedances, while careful attention to layout is required to minimize coupling of the digital outputs into the sensitive analog input.

In fact, good layout is paramount to maintaining ADC performance, yet ever more demanding market requirements call for smaller designs and higher channel density, which exacerbate layout issues. These design requirements can challenge even the most seasoned engineer if his expertise lies in the RF or digital worlds.

The LTM9002 dual-channel, IF/baseband receiver harnesses years of applications design experience and squeezes it into an easy-to-use 11.25mm × 15mm µModule package. Inside the package is a high performance dual 14-bit ADC sampling up to 125Msps, antialiasing filters, two fixed gain differential ADC drivers and a dual auxiliary DAC. By combining these components, the LTM9002 eliminates the burden of input impedance matching, filter design, gain/phase matching, isolation between channels and high frequency layout, dramatically improving time to market. Even in this small package, the LTM9002 guarantees high performance that will enhance many communications and instrumentation applications.

Multichannel ADC Applications

Multichannel applications have several unique requirements, such as channel matching in terms of gain, phase, DC offset, and channel-to-channel isolation. Gain and phase errors directly affect the demodulation of the I and Q channels. And since direct conversion receivers are typically DC-coupled, DC offset limits the dynamic range of the receiver. Multiple-input, multiple-output (MIMO) systems depend on multiple receiver channels all receiving the same signal while detecting the slight variations caused by multipath delays so gain and phase errors affect these systems as well. Like I/Q receivers, diversity receivers require excellent isolation between channels because crosstalk appears as noise corruption and can be more difficult to suppress

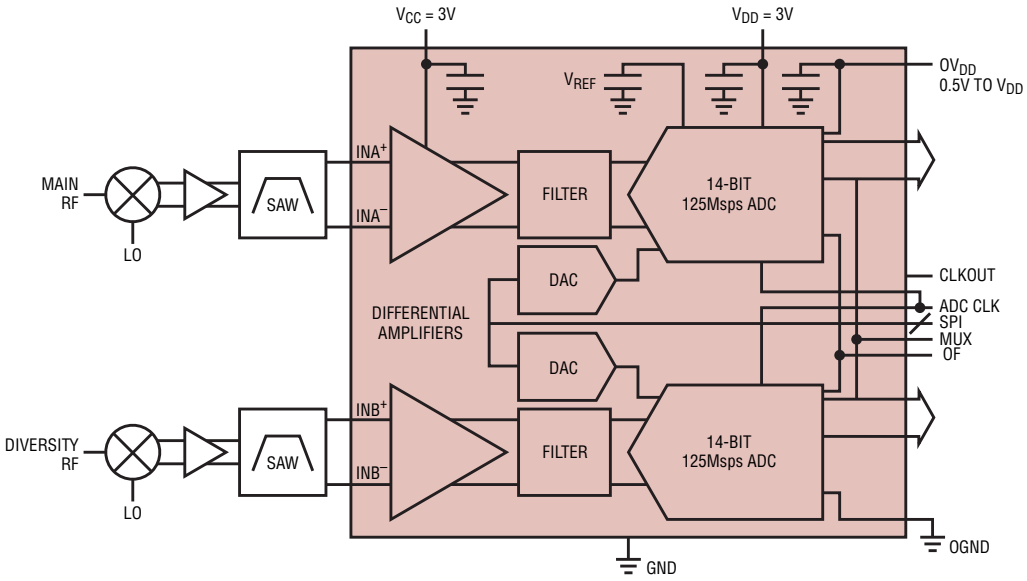


Figure 1. LTM9002 used for a Main/Diversity receiver.

with digital filtering. Clearly, channel matching and channel isolation of the ADC and driver circuits directly impact system-level performance. For many multichannel applications, these errors cannot be corrected in the digital domain.

Performance

The LTM9002 achieves 66dB Signal to Noise Ratio (SNR) and 74dB Spurious Free Dynamic Range (SFDR) at 140MHz input frequency. Figure 2 shows the FFT under these conditions. SNR is a function of the ADC and amplifier performance as well as the amplifier gain and filter bandwidth. The inherent amplifier noise is proportional to the voltage gain; therefore, the 26dB amplification increases the amplifier noise by 20 times whereas 8dB amplification would only increase the noise by 2.5 times. Likewise, the amplifier noise (in nV/$\sqrt{Hz}$) increases with the square of the filter bandwidth. It is important to remember these relationships when assessing the entire signal chain.

For multichannel applications, channel-to-channel matching and isolation are important considerations. The LTM9002 achieves 90dB isolation at 140MHz input frequency despite the small form factor. The overall gain is typically 26dB on the default span setting and varies just 0.1dB between the two channels. The 12-bit auxiliary DAC can be configured to adjust the span by 61µV per step using the circuit in Figure 3.

Another important performance metric is printed circuit board (PCB) area efficiency. Here, the LTM9002 excels. The LTM9002 requires no external components—no supply bypass capacitors, no passive filtering, no impedance matching or translating components. In many IF-sampling applications, gain can be obtained through transformers, but they are often large and difficult for automated assembly equipment to mount. In DC-coupled applications, amplifiers are required as ADC drivers, along with their associated antialias filter network. It is not uncommon for the entire IF/baseband receiver system to consume two square inches of board area (approximately 25mm × 50mm). None of this external circuitry is required with the LTM9002 so it requires only about one-quarter of a square inch (11.25mm × 15mm), better by a factor of eight.

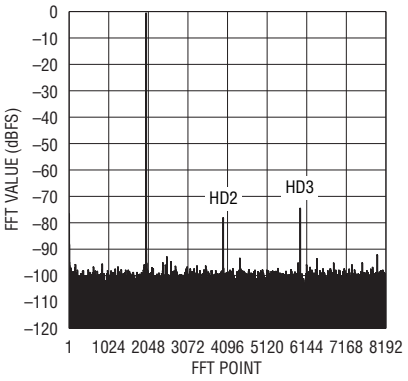


Figure 2. FFT showing LTM9002 AC performance with 140MHz input frequency.

Attributes and Configurations

The µModule construction allows the LTM9002 to mix standard ADC and amplifier components regardless of their process technology and match them with passive components for a particular application. The µModule receiver consists of wire-bonded die, packaged components and passives mounted on a high performance, 4-layer, Bismaleimide-Triazine (BT) substrate. BT is similar to other laminate substrates such as FR4 but has superior stiffness and a lower coefficient of thermal expansion.

The LTM9002-AA utilizes a dual, 14-bit, 125Msps ADC, two 26dB fixed-gain amplifiers and also includes a 12-bit dual DAC configured for full-scale span adjustment as shown in Figure 1. Internal antialias filters limit the input frequency to less than 170MHz. The amplifiers present a 50Ω differential input impedance and an input range of ±50mV, or –16dBm. This default span is set by connecting the SENSE pin to V_{DD}, and can be adjusted in three ways. For a –3dBm lower span, the SENSE pin can be connected to 1.5V. By connecting SENSE to V_{DD} or 1.5V, the internal reference is used. An external reference can be used by applying 0.5V–1.0V to the SENSE pin. The auxiliary DAC offers a final option for selecting the range. Alternately, fine adjustments to the span, such as balancing the gain of the two channels, can be made with external references or the auxiliary DAC.

Multiple power saving modes include independently disabling either amplifier or the ADC. The ADC has two shutdown states: NAP and SLEEP modes. In NAP mode, the internal reference remains biased so that conversions can resume within 100 clock cycles upon start-up. In SLEEP mode the reference is shut down and start-up takes 1µs or more. A clock duty cycle stabilizer feature is available and an output clock signal is provided for accurately latching the output data. The two channels can be

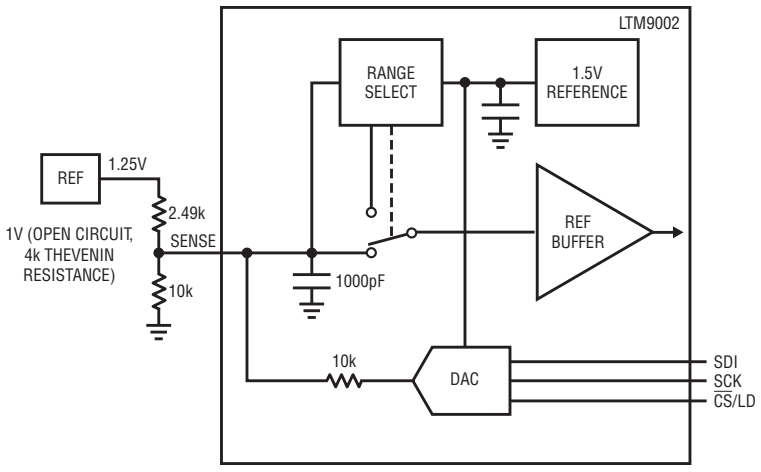


Figure 3. Using an external reference and the internal auxiliary DAC for span adjustment.

output on separate parallel busses or multiplexed onto a single parallel bus to save processor pins.

Interfacing to the Analog Inputs

The analog inputs of the LTM9002 present a differential 50Ω resistive input impedance, which in most cases exactly matches the signal path. The input common mode level should be approximately $V_{CC}/2$. Traditionally, the input of an ADC requires considerable care in terms of drive current, settling time and response to the nonlinear characteristics of sample-and-hold switching. For lowest distortion performance, the common mode level at the ADC inputs must be optimized for the particular ADC front-end; for best signal-to-noise (SNR) performance, the signal swing must utilize the maximize ADC input range. All this is taken care of within the LTM9002.

Interfacing to the Digital Outputs

The LTM9002 uses standard CMOS output buffers that switch from OV_{DD} to OGND. OV_{DD} can range from 0.5V to 3.6V, accommodating many different logic families and OGND can be as high as 1V. Because the LTM9002 supplies are internally bypassed, no local supply bypass capacitors are required. The power supply for the digital output buffers should be tied to the same supply that powers the logic being driven. For example, if the converter drives a DSP powered by a 1.8V supply, then OV_{DD} should be tied to that same 1.8V supply. Lower OV_{DD} voltages also help reduce interference from the digital outputs to the analog or clock circuitry. OV_{DD} and OGND are isolated from the ADC power and ground. An internal resistor in series with the output makes the output appear as 50Ω to external circuitry and may eliminate the need for external damping resistors.

Power Supplies and Bypassing

The LTM9002 requires a 3.0V supply. To optimize performance for each block within the LTM9002, multiple supply pins are used. Internally, each supply is bypassed to ground very close to the die to minimize coupled noise. A common problem with traditional ADC board layouts is long traces from the bypass capacitors to the ADC degrade system performance. The bare die construction with internal bypass capacitors in the LTM9002 provides the closest possible decoupling and eliminates the need for external bypass capacitors.

Conclusion

Multichannel ADC applications need good channel-to-channel matching and isolation without consuming valuable board space. Driving high performance ADCs is challenging enough without the matching, isolation and board space constraints. The LTM9002 integrated dual IF/baseband receiver subsystem manages to address all of these requirements while eliminating the design task of mating an ADC and its driver. By integrating the passive filtering and supply bypassing, the overall size is dramatically smaller than otherwise possible with discrete implementations. The LTM9002's µModule packaging is itself developed to maximize the performance of the integrated components.

LTC4350, continued from page 9

Specifics of Power System Design With a Bidirectional Energy Flow Power Supply

Certain switcher topologies, such as a synchronously rectified buck converter, permit large, uncontrolled reverse current if the output voltage is forced to a potential that is higher than the regulation point. In addition, an unwelcome transient can occur when one LTC4350 power channel is added to an operating system. Due to the difference between the initial power supply output voltage and the operating output voltage (usually 200mV–300mV), significant negative current can be induced in the newly added power supply. This current can disable the LTC4350 if the voltage drop at R_{SENSE} exceeds 50mV. After the negative current drops, the LTC4350 goes into its initial start-up cycle and the process may repeat indefinitely. This current can also damage the power supply, as it does not have the ability to transform energy to the primary side.

An equivalent output power stage circuit that exemplifies this case is shown in Figure 10.

To reduce or eliminate negative current, it is necessary to reduce the difference between voltages when the MOSFET switch is first turned on. The newly activated power supply output voltage starts to increase when the LTC4350 load share capability is brought into operation. The LTC4350 is designed to launch the load share mechanism when the gate pin voltage exceeds V_{CC} by 4V but the MOSFET's gate threshold is in the range of 1V to 5.5V. To synchronize both events, activating load share capability and turning on the power switch, the MOSFET threshold voltage must be higher than or equal to 4V. This is easily satisfied by using a sub-logic level MOSFET and placing a low knee current Zener diode (Central Semiconductor's CMPZ4676-CMPZ4682) in the MOSFET gate circuit.

An alternative solution involves disabling synchronized rectification until the LTC4350 STATUS pin signal is low and load share capability is active, but this method is restricted by the power supply controller's ability to power up non-synchronously in a condition of unidirectional energy flow.

Conclusion

The calculations and methods described here show how the LTC4350 can be used to build a stable and accurate load share power system with any kind of power supply, including a mix of power modules. The LTC4350 also has the unique feature of operating with bidirectional power flow converters.

Battery Manager Enables Integrated, Efficient, Scalable and Testable Backup Power Systems

by Mark Gurries

Introduction

Customers of information management systems demand a guarantee that critical data is always safe. Redundant data storage systems and data backups preserve data once it is written to persistent media such as disk or tape, but data stored in cached RAM is vulnerable in the face of a power failure. Some systems always have a significant amount of data in RAM, and in a complete power loss, this data is lost. The typical solution to preserving transient data is an uninterruptible power supply (UPS), which provides AC power to the entire system. The drawback to this method is that it is not easily scalable—one oversized and expensive system must cover all scenarios.

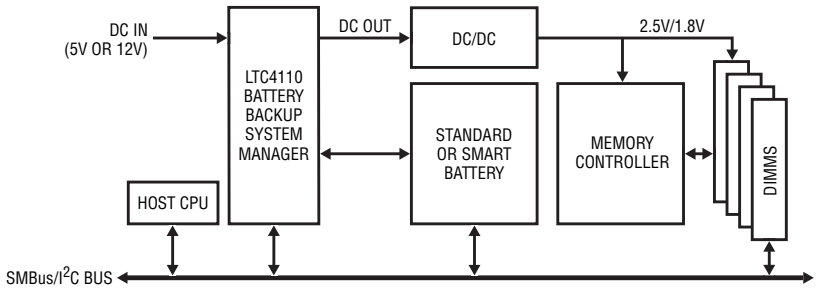


Figure 1. Block diagram of LTC4110 in a CPU/server system

Varying Scales of Battery Backup

The scale of the battery backup ranges from an entire system of multiple information products working together to smaller, self contained products. In the case of the large system, the system must remain running until it has had time to properly save the data and then shutdown. Often this means everything connected to the system must also remain alive. In short, the battery backup system must support the entire system while it running full blast. If the data of concern is contained entirely in the CPU processor, then naturally the size of the battery back up system scales down appropriately.

AC Backup is Inefficient

As mentioned in the introduction, the typical approach to solving the transient data problem is to supply power to the entire system via its AC input. Unfortunately, AC-level backup requires inefficient power conversions from DC to AC and back to DC, thus assuring a relatively large battery capacity for a given backup time. This is good for battery manufacturers, but bad for systems customers. The result is a physically huge and very expensive third party UPS battery backup system that must be capable of supplying worst case power consumption levels at worst case efficiencies.

The current third-party UPS paradigm takes profits that should be in the pockets of information system vendors and puts them into the pockets of UPS vendors.

A new paradigm places compact, tightly integrated, efficient and cost-effective battery backup solutions directly into the information system. The integrated system offers features and performance beyond the abilities of any UPS system.

Poorly Integrated Solutions

As is often the case, these information systems were never designed with battery backup in mind, which is one of the big reasons why AC backup is used. The lack of interoperability between the battery backup and the data system means it is difficult to optimize the complete system to save money, manage energy or generate status reports on what is really going on. The solution looks and acts like it is a cumbersome afterthought, which it is. In an extreme contrast, the every day notebook computer is an excellent example of what could be achieved in integrated power management.

The False Perception of High Cost

The consequence of traditionally large and expensive UPS solutions is that it limits the market opportunity for a system builder to offer battery backup as a built-in feature. Customers must weigh the advantages of a UPS against its reputation as a mini power station, often rationalizing ways to avoid it. Low demand drives down the incentive for system designers to integrate a UPS system. Unfortunately, this type of thinking shuffles profits into the UPS vendor's pocket that should be in the pockets of the information system vendors.

The reality is that a compact, tightly integrated, efficient and cost-effective battery backup solution can be designed directly into the information system, and it can offer features and

performance beyond the abilities of any UPS system. First of all, there is a huge reduction in power needed since the backup power can be directed just to those circuits that need to be kept alive. Likewise, there are no AC efficiency losses to deal with. The combined power savings significantly reduces the physical size of the battery, making it possible to fit the entire battery backup system inside the product chassis. To address scalability issues, the integrated battery backup concept can be extended to other parts of the information system as required if multiple points of data need to be protected.

New Competitive Edge

By integrating battery backup into the information system, an information system vendor can offer better monitoring and reporting functions than a third party UPS system at a significant overall *cost savings* to the customer. This is a competitive advantage, as it is a clear win for both the system designer and the customer.

The Challenge

If the information system's design engineer is to integrate a reliable backup system as an extension of the product, there are some technical challenges encountered right up front. There are three basic subsystems involved in a complete solution.

- ❑ Battery charger
- ❑ PowerPath management
- ❑ Status reporting

These subsystems are readily available as separate integrated devices, but what if you want features that require these systems to work closely together? For instance, knowing and maintaining the battery's health and state of charge at all times in all conditions requires the concerted effort of all three systems. Other desirable features in a battery backup system include:

- ❑ Good battery verification to eliminate backup failure surprises.
- ❑ Scalability as the system grows.
- ❑ Efficiency to keep the box cool.
- ❑ Redundancy support for customers with contracts guaranteeing no data loss.
- ❑ Retain failure status even when the battery has failed, to prevent a false sense of security.

Table 1. LTC4110 battery pack charge mode capabilities

Parameter	Chemistry			Maximum Charge Time (SLA excluded)
	Li-ion	NiMH or NiCd	SLA/ Lead Acid	
Standard Battery Support	✓		✓	Adj. up to 12 Hours
Smart Battery Support	✓	✓	✓	Unlimited

Complete Backup Battery Manager

The LTC4110 makes it possible to implement a reliable, efficient and scalable battery backup system by integrating the following functions in a single IC:

- ❑ **An efficient multi-chemistry standard and smart battery charger:** No need to burden processor with charging task.
- ❑ **Automatic PowerPath management:** Offers smooth switching between all power sources.
- ❑ **Flexible status reporting:** Status of all modes and faults over SMBus.
- ❑ **Gas gauge support:** Supports both Smart Battery and simple capacity verification for standard batteries.
- ❑ **Test load the battery:** Verify it is still good so there are no surprises.
- ❑ **Scalability:** Able to add more LTC4110's to increase total available battery capacity.
- ❑ **Efficiency:** Synchronous rectification, low loss FET ideal diode and zero heat test loading battery.
- ❑ **Redundancy support:** Use multiple LTC4110's in parallel to provide full single fault tolerance.
- ❑ **Flexible I/O pins:** Use definable GPIO pins or status output pins.
- ❑ **Status retention:** Retains battery backup failure status after battery has died.

This is only a summary of features. Let us look at an example application to see how all of these features come together.

The LTC4110's Tightly Coupled Architecture

Figure 1 shows how the LTC4110 fits into a battery-backed-up server memory system. The LTC4110 connects to the existing I^2C bus, thus leveraging existing communication infrastructure. It stands between the main distribution supply and the memory system power supply, ready to cut in the battery when the input fails.

Table 2. The LTC4110's battery pack charge voltage capabilities

Chemistry	V_{CELL} Full Charge (V)	V_{CELL} Adj. Range (V)	Series Cell Count	Nominal Stack Voltage (V)
Lead Acid	2.35	±0.15	2, 3, 5 & 6	4, 6, 10 and 12
Li-ion	4.2	±0.3	1, 2, 3 & 4	3.6, 7.2, 10.8 and 14.4
NiMH or NiCd	N/A	N/A	4, 6, 9 &10	4.8, 7.2, 10.8 and 12
Super Caps	2.5, 2.7 or 3	Yes	2 to 7	5 to 18

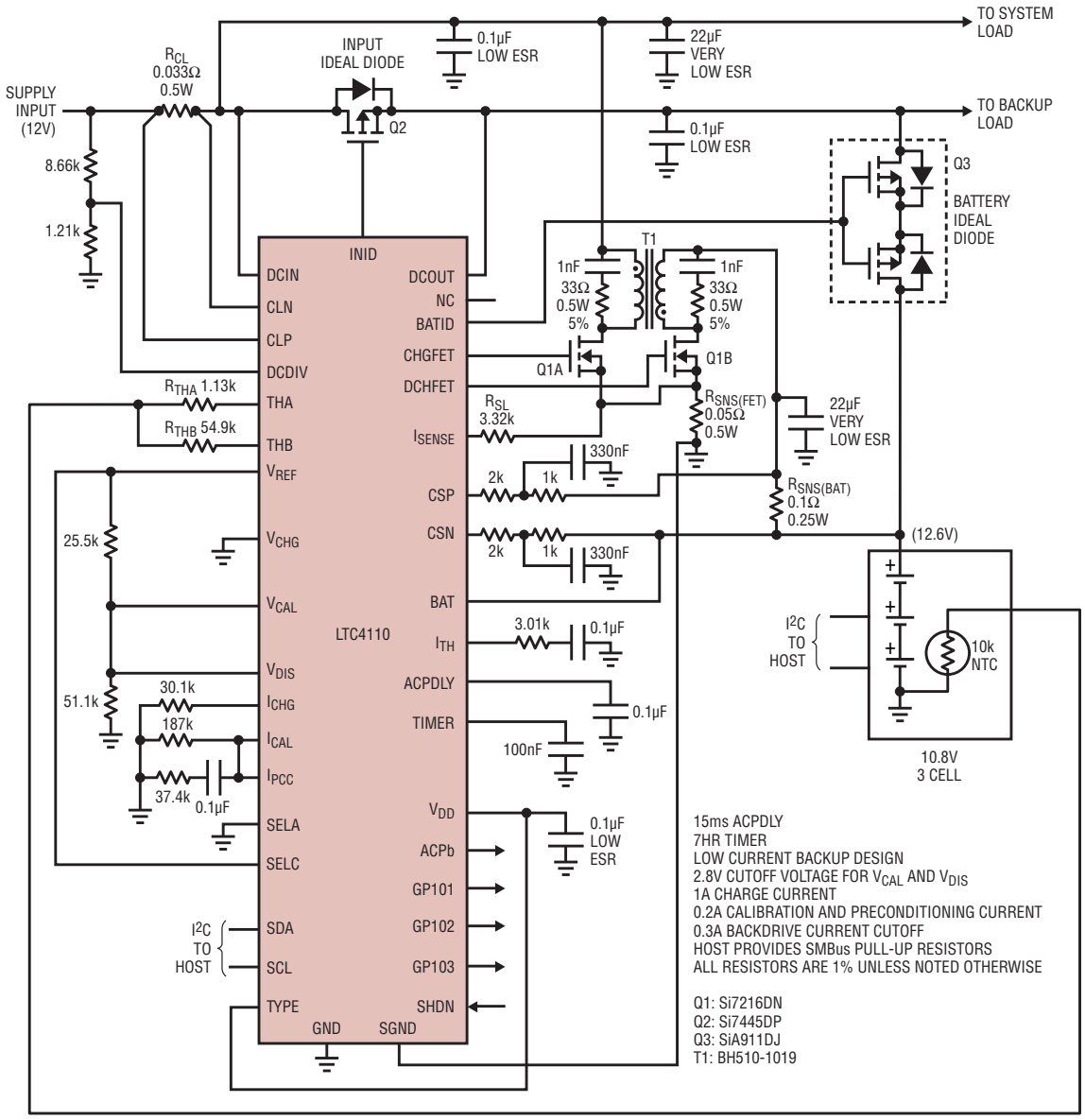


Figure 2. A LTC4110-based battery backup system

It isolates DCIN from DCOUT so that the only load the battery is supporting is memory. The existing DC/DC converter converts the unregulated battery voltage and continues to provide the regulated voltage to the memory.

Figure 2 shows the LTC4110 battery backup controller schematic. The schematic shows a 12.6V Li-ion being charged from a fixed 12V power source.

Super Flexible Battery Charger

The 300kHz battery charger consists of an efficient synchronous rectified flyback charger with an input range of 4.5V to 19V intended for charge rates of up to 3A. The wide 2.7V to 19V output voltage range is capable of charging batteries to full termination voltage whether the voltage is less than or greater than the input supply voltage. There is no need to configure the battery pack voltage to work within the limits of the input supply, thus giving you total freedom to optimize the battery for the application. For batteries that use constant voltage charge, the output accuracy is ±0.5%, but at the same time adjustable allowing you to optimize a battery for longer battery life or maximum capacity. Float voltage temperature compensation is also offered for sealed lead acid batteries.

The LTC4110 contains many battery charge protection systems, including charge-preconditioning qualification for all chemistries before entering bulk charge and a thermistor interface to monitor battery temperature. Safety timers are also used in various ways to prevent battery overcharge or to help detect defective batteries. If a battery faults, charge status is updated. In Standard Battery mode, the LTC4110 uses built in charge termination capabilities. In Smart Battery mode, the battery itself controls charge termination. Regardless of the mode, the battery charger is capable of charging many different types of battery chemistries in many different

cell configurations. Tables 1 and 2 provide a quick overview of the LTC4110 charge capabilities. Figure 3 shows the power flow in charge mode.

Building Confidence in Your Battery While Keeping Your Cool

Knowing the condition of the backup battery at all times is essential if one is to have any confidence in the system. Under the watchful eye of a host CPU or power manager, there are three things you can do to build that confidence:

- ❑ **Test loading the battery:** Does the battery still work?
- ❑ **Verify battery capacity:** Does it still have the retained capacity to support the backup?
- ❑ **Gas gauge status:** What is the State of Charge (SOC) of the battery?

Test loading the battery at first seems straightforward enough. Simply connect a test load to the battery and watch it work. Ideally, the battery is tested while in the product, avoiding the need to open up the box. The big issue one must deal with is the heat the load generates during the test. In many applications, the product itself is already operating close to thermal limits, which means putting that extra heat inside the box may not be possible.

In LTC4110 terms, test loading the battery is part of a mode called "calibration." In calibration mode, the LTC4110 uses its flyback charger in reverse to discharge the battery with a programmable constant current into the "system load" eliminating heat generation. During calibration, the main AC/DC power supply simply sees a reduction in the system load current equal to the current provided by the battery. There is no temperature change inside the product. The battery continues to discharge until conditions are met to terminate discharge. Upon termination of discharge, the LTC4110 automatically starts a recharge cycle to return the battery back to ready status. Figure 4 shows the power flow in calibration Mode.

Verifying battery capacity can be easily done during the same calibration process. With a battery discharge current accuracy of ±3% at $R_{SNS(BAT)}$ in Figure 2, the host can start the calibration process while monitoring the elapsed time it takes for the full battery to reach empty. The host, knowing the fixed load current, can use the time information to determine the battery's present storage capacity (amp-hour) with reasonable accuracy.

If one desires to have full time high accuracy battery SOC monitoring, the industry standard Smart Battery System (SBS) Gas Gauge, as found in every notebook PC made today, is the only real solution. The LTC4110 fully supports this standard in charge, discharge and calibration modes of operation.

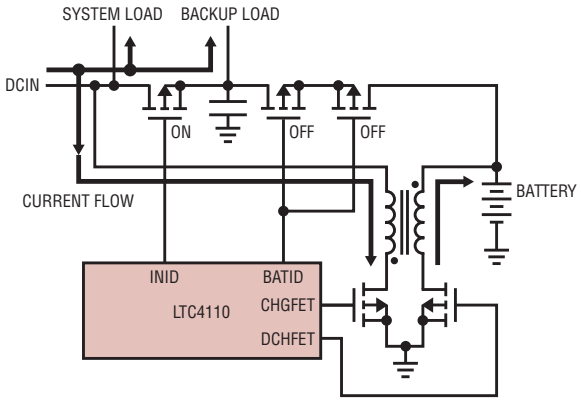


Figure 3. The LTC4110 in charge mode

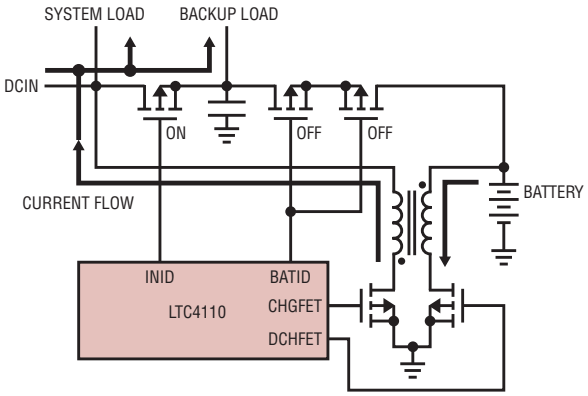


Figure 4. LTC4110 in calibration mode

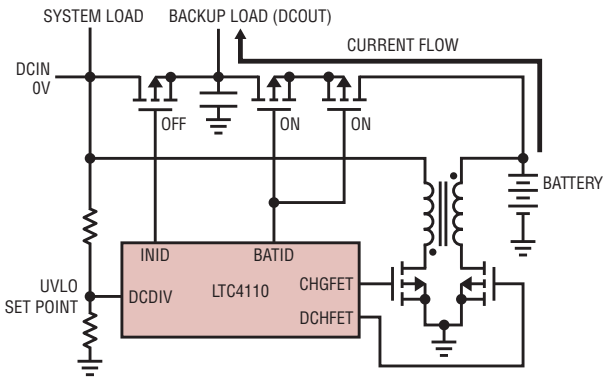


Figure 5. The LTC4110 in battery backup mode

Lossless Automatic PowerPath Operation

The LTC4110 uses ideal diode circuitry to drive its PowerPath™ MOSFETs. An ideal diode circuit uses a MOSFET where normally a diode would be used to control the flow of power. Like a true diode, current is only allowed to flow in one direction despite the fact that MOSFETS can conduct current in both directions. The forward voltage drop of an ideal diode is far less (25mV) than that of a conventional Schottky diode (350mV), and the reverse current leakage can be smaller for the ideal diode as well. The tiny forward voltage drop reduces power losses, minimizes self-heating and ,in the case of a battery, extends battery life.

In Figure 2, there are two sets of ideal diodes forming a power-OR between the supply input (DCIN) and the battery, forming an output called *backup load* (DCOUT). In the Figure, two back-to-back MOSFETs are used in the battery path since in this application the full charge battery voltage is greater than the DCIN voltage. However, if the battery voltage is less than DCIN, only one MOSFET is needed.

Under normal conditions, the input ideal diode is always on. If the DCIN voltage divider senses a condition where battery backup is desired, the battery ideal diode is turned on with the input ideal diode left to figure out when to turn off on its own. The diode action allows the highest supply to take up the backup load. But since DCIN is falling, the input ideal diode turns off as soon as it senses a reverse current flow. The goal of the ideal diode design is to always attempt to do a "make before break" handover if possible, minimizing the need for any "bridging" or "holdup" capacitance. Figure 5 shows the LTC4110 in battery backup mode. The thick line shows the active power path.

Expandable Capacity or Creating Redundancy

Ideal diode technology is also the key that allows one LTC4110 to work with other LTC4110s in safely paralleling batteries for redundancy. Multiple LTC4110s can be connected in parallel at the backup load (DCOUT) point. At no time will the batteries exchange current between them regardless of any difference in SOC or voltage.

Assuming the batteries are the same make, model and age, the batteries automatically act as one big battery, sharing discharge load current based on their relative SOC ratios. If all the batteries are the same SOC, the current is equal among them. Charge current remains independent.

Some battery chemistries, such as Li-ion, have rules about the size of the battery that can be safely transported. If your backup needs exceed 95 watt-hours of capacity, you must use multiple batteries. Simply add another LTC4110 to support dual battery operation. Fortunately, this expansion also gives the system true redundancy by minimizing the number of parts shared between each backup system. Figure 6 shows a dual LTC4110 system using two standard (not Smart) batteries.

Flexible SMBus Addressing and Registers

Whether you are using Smart Batteries or standard batteries, the LTC4110 supports an SMBus interface that the host CPU can use to control and monitor each part. To make configuration easier with standard batteries, the LTC4110 supports up to three unique SMBus addresses. However, if you use Smart Batteries, all of the LTC4110s must use the same address and each LTC4110 and associated Smart Battery local SMBus must be isolated from all the other LTC4110s. This is easily done with SMBus multiplexer such as the LTC4305 or LTC4306 under the control of the host CPU. Wherever possible, the LTC4110 follows the Smart Battery System (SBS) Charger Specification for registers definitions for compatibility with software that works with Smart Batteries.

Complete Status and Flexible GPIO Lines

Internally, the LTC4110 uses two 16-bit SMBus read registers to report 27 unique status items. This includes a bit that retains and reports if the battery backup has failed, even after the battery has gone below the user defined end of discharge cutoff (dead) threshold. Another 16-bit SMBus write register controls the charger and how the three GPIO bits are to be used.

Each GPIO bit can be programmed to report selected internal status information or work as generic digital I/O independently of the other bits. A fixed AC present status output bit is offered

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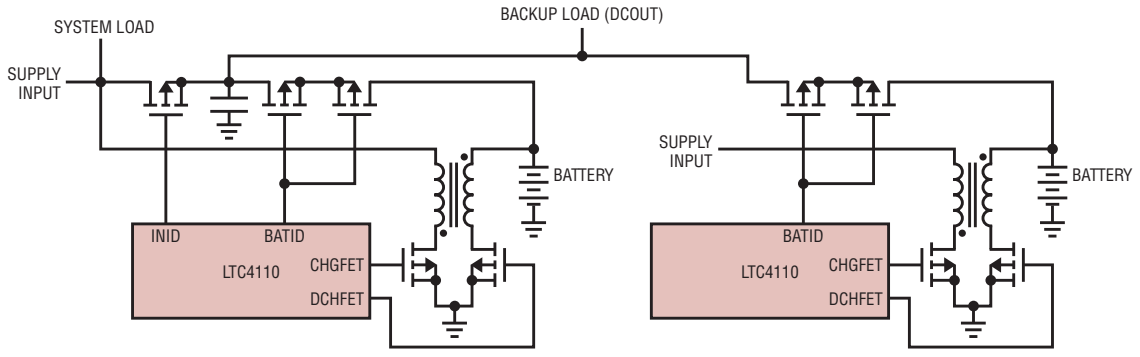

Figure 6. Dual LTC4110 system using standard batteries

500nA Supply Supervisors Extend Battery Life in Portable Electronics

by Bob Jurgilewicz

Introduction

Power consumption is an important concern in the design of electronic devices, particularly battery-powered products. The challenge facing a device designer is how to add features without significantly degrading the device's battery run time. For instance, take apart any modern portable device and you will find a number of integrated circuits that draw some current even when they are idle. It is important to minimize both quiescent and operating currents of the embedded circuits to maximize the operating battery life of the application.

Sometimes, under weak battery conditions, you may turn on a device only to find it unresponsive and partially configured after premature termination of its power-on sequence. One way to avoid this is to monitor the system power with supply supervisors that require very little power, allowing them to respond even when a battery is significantly drained. The LTC2934 and LTC2935 ultra-low power supervisors provide accurate voltage monitoring and microprocessor control during all phases of equipment operation. System initialization, early power-fail warning, manual reset and power-on/off reset generation are all included, requiring a scant 500nA from your power source.

While ideal for battery powered products, the LTC2934 and LTC2935 can be used in any system requiring voltage monitoring and/or microprocessor control. The supervisors' ultra-low load current allows products to use smaller batteries and have longer operating life. Typical applications include portable data-loggers, medical devices, remote systems and intrinsically safe equipment.

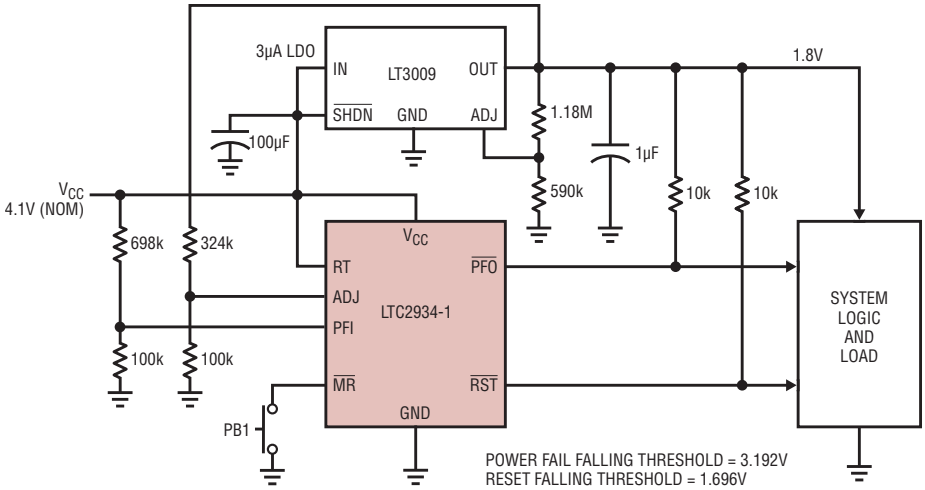

Figure 1. Typical supply monitor application

Under weak battery conditions, you may turn on a device only to find it unresponsive and partially configured after premature termination of its power-on sequence.

One way to avoid this is to monitor the system power with supply supervisors that require very little power, allowing them to respond even when a battery is significantly drained.

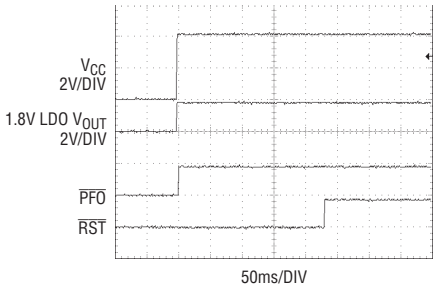

Figure 2. Typical power-up waveforms

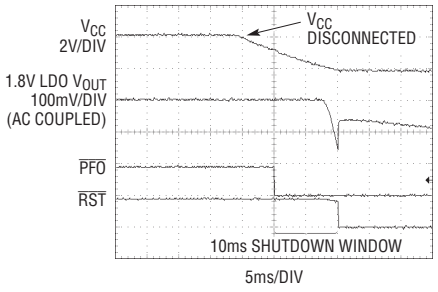

Figure 3. Typical power-down waveforms

Rising Supplies: Start-Up is Im-POR-tant

It is important to control the start-up of devices as power supplies come online. The LTC2934/35 power-on reset (POR) function provides voltage monitoring and logic control to prevent starting a microprocessor at insufficient supply voltage. The POR function also generates a time delay to provide some margin for supply voltage settling. This time delay also allows a processor oscillator to build up and reach a stable frequency before permitting the microprocessor to execute code.

The reset output ($\overline{RST}$) from the supervisor typically connects to the reset input of the microprocessor. During system start-up, the supervisor holds the $\overline{RST}$ output low. Once the voltage reaches a prescribed minimum value, the internal reset timer begins to run, holding the $\overline{RST}$ output low for an ad-

ditional time (typically 200ms). When the reset timer expires, the $\overline{RST}$ output pulls high and releases the microprocessor from its reset condition.

Figure 2 shows the supply rising waveforms obtained from the typical application shown in Figure 1. When V_{CC} exceeds the power-fail threshold plus 2.5% hysteresis (3.192V × 1.025 = 3.272V), the power-fail output ($\overline{PFO}$) is allowed to pull high. The LT3009 (a 3µA LDO) is powered from V_{CC}. Since the $\overline{PFO}$ output is pulled up by the LDO output, $\overline{PFO}$ will follow the LDO. When the LDO output exceeds the reset threshold plus 5% hysteresis (1.696V × 1.05 = 1.781V), the internal reset timer begins to run. After 200ms, $\overline{RST}$ pulls high and system logic connected to $\overline{RST}$ is released from its reset condition.

Falling Supplies: Heed the Early Warning

Unmanaged power loss can cause many system problems. The LTC2934 and LTC2935 contain a power-fail logic output ($\overline{PFO}$) that pulls low to provide an early warning of impending power loss. To be useful, an early warning should occur before the monitored supply falls to insufficient levels and well before the $\overline{RST}$ output pulls low. The time between $\overline{PFO}$ and $\overline{RST}$ pulling low can be used to initiate a variety of critical operations prior to shutdown. Once the supervisor pulls the microprocessor reset low, it may be impossible to execute operations. Operations initiated by a power-fail warning include shutting off non-critical components to conserve energy and writing important data to memory. Some secure applications may also require erasing data to thwart memory snoopers.

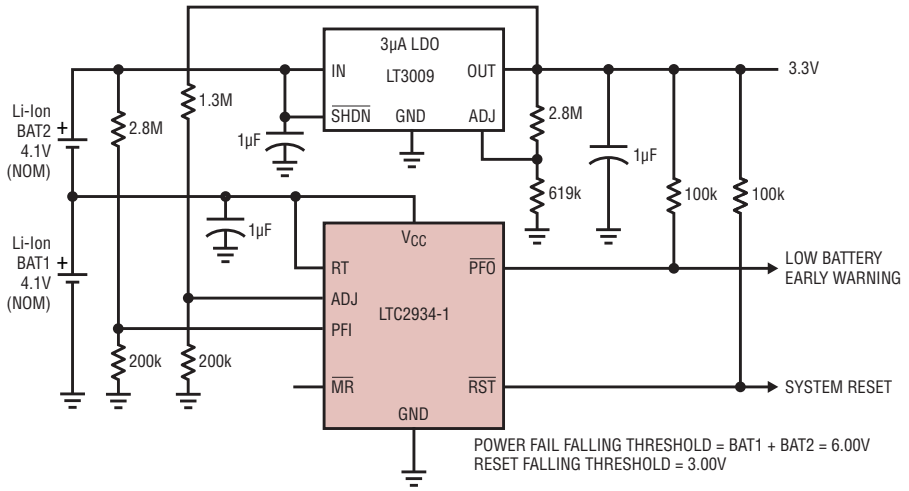

Figure 4. Stacked Li-ion cell and LDO supervisor

Figure 3 shows the supply falling waveforms obtained from the application shown in Figure 1. The waveforms demonstrate how $\overline{PFO}$ provides ample warning when V_{CC} is suddenly disconnected from the system. The LT3009 supplies a constant 10mA to a load at 1.8V. The 100µF input capacitor begins to discharge when V_{CC} (4.1V nominal) is disconnected. The power-fail threshold is configured for 3.192V.

Because the power-fail condition persists and is not merely transitory, logic output $\overline{PFO}$ pulls low and remains low after a small comparator delay. This is when the system logic (typically connected to $\overline{PFO}$) should take appropriate shutdown action(s). In this application, the remaining operating time beyond power fail is approximately 10ms. Eventually V_{CC} becomes so low that the LDO begins to drop out. $\overline{RST}$ asserts low shortly after the LDO output falls below the reset threshold (1.696V). At this point, the system load is removed and the LDO output begins to recover. However, the remaining loads and built-in hysteresis prevent the LDO recovery from glitching the $\overline{RST}$ output.

Table 1. Falling threshold selection table

Reset Threshold (V)	Power-Fail Threshold (V)	S1	S2	S0
3.30	3.45	Low	Low	Low
3.15	3.30	Low	Low	High
3.00	3.15	Low	High	High
2.85	3.00	Low	High	Low
2.70	2.85	High	High	Low
2.55	2.70	High	Low	Low
2.40	2.55	High	Low	High
2.25	2.40	High	High	High

Select Fixed or Adjustable Thresholds

The LTC2935 integrates eight precision reset and power-fail threshold pairs. Configure any one of the eight threshold pairs using three digital select inputs (see Table 1). Typical applications using the LTC2935 require no additional external components. As a result, solutions require little board space and are extremely low power.

Use the LTC2934 when custom (adjustable) thresholds are necessary. The LTC2934 monitors voltage applied to its PFI and ADJ inputs, typically through an external resistive divider. External divider resistance values can be large which helps keep the current low. Divider errors due to input leakage current (1nA maximum over temperature) are often too small to worry about. The PFI and ADJ inputs have precision 400mV thresholds

(falling), so low voltage monitoring is possible.

The falling threshold accuracy for both the LTC2934 and LTC2935 is ±1.5% over the full operating temperature range. Minimum V_{CC} is a low 1.6V. Configuration details are discussed in the LTC2934 and LTC2935 data sheets.

Manual Reset and Reset Timing

The LTC2934 has two selectable reset timeout periods. Tie the RT input low for a 15ms timeout. Tie the RT input high for a 200ms timeout. The LTC2935 has a fixed 200ms timeout. Both parts have a manual reset input which asserts $\overline{RST}$ low when the $\overline{MR}$ input is pulled low (typically with a switch). The $\overline{MR}$ input has an internal 900k pull-up resistor to V_{CC}, used to pull up the $\overline{MR}$ input when the switch is open. Alternatively, the $\overline{MR}$ input may be pulled low with an external logic signal. When the $\overline{MR}$ input returns high, $\overline{RST}$ pulls high after the reset timeout period has elapsed, assuming that the monitored input voltage is above the reset threshold.

Monitoring a 2-Cell Li-Ion Stack

Some portable applications utilize a stack of batteries to achieve greater product operating lifetime. For a product using two stacked 4.1V Li-ion cells (or similar), the total stack voltage (8.2V) exceeds the maximum operating voltage (5.5V) of the LTC2934. However, if the center tap of the 2-cell stack is available, cell monitoring is still possible. Figure 4 shows how the center tap of the stack is used to bias the LTC2934. The total stack voltage is monitored at the power-fail input (PFI). The application is configured to pull the $\overline{PFO}$ output low when the sum of the battery voltages drops below 6.00V. The adjustable input (ADJ) monitors the LDO output. $\overline{RST}$ pulls low when the LDO output drops below 3.00V.

Super Hysteresis

Some applications have a large load transient when powered. This transient can cause significant supply voltage drop if battery series resistance is large. If the load is enabled after the reset output pulls high, the subsequent voltage drop could put the voltage at the V_{CC} monitor input below threshold, causing the reset and power-fail outputs to pull low. In such cases, active threshold control (shown in Figure 5) is helpful. The LTC2935 power-fail output ($\overline{PFO}$) can be used to change any (or all) of the threshold control input states (S2, S1, S0). The power fail comparator threshold is always 150mV larger than the reset threshold and the power-fail output does not experience the 200ms reset timeout delay. If the power-fail output pulls high before the reset output (which is almost always the case with rising supplies), it can then be used to lower the falling thresholds to one of the other seven threshold selections. In Figure 5, the reset falling threshold is changed from 3.3V ($\overline{PFO}$ low) to 2.25V ($\overline{PFO}$ high), which provides a generous 1.05V of falling hysteresis.

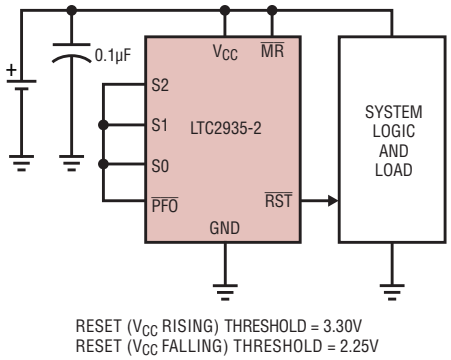

Figure 5. Active threshold control

Conclusion

The 500nA current required by the LTC2934 and LTC2935 supervisors is so small, it can be placed into the "Don't Care" column of your device power budget. Although the power is low, these supervisors don't discard features. The power-on reset and early power-fail warning signals provide glitch-free logic controls to your system logic. Reset delay time is built in. Manual reset is available in both parts. Configuring these supervisors is easy, and few if any external components are necessary. Ultra-low input leakage specifications make high impedance applications possible. Specifications are guaranteed from –45°C to 85°C. Both parts are available in space saving 8-lead, 2mm × 2mm DFN and TSOT-23 (ThinSOT™) packages.

LTC4110, continued from page 21

at all times. However, if you do not have SMBus in the product, the LTC4110 can be configured to enable preset status information to drive the GPIO bits on power up. This information can be used to drive status LEDs.

Micropower Shutdown and Shipping

The LTC4110 shutdown pin is designed to prevent false shutdowns on power up or power down. Reading the pin status is pre-qualified such that it is only honored under normal conditions. This qualification allows the product to ship with the battery installed without fear of the part entering into battery backup mode and draining the battery. The shutdown current only draws 20µA from the battery. This is the same shutdown mode that the LTC4110 enters when the backup battery reaches its end of discharge point.

Conclusion

The LTC4110 is a flexible standalone battery backup controller. By integrating key features into a single IC, functions work together seamlessly, allowing the designer to offer a reliable and complete battery backup system with minimal design effort.

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Quad Output Regulator Meets Varied Demands of Multiple Power Supplies

by Michael Nootbaar

Introduction

Many modern electronic devices require a number of power domains to satisfy the needs of a wide variety of devices and subsystems. A power supply designer's job would be relatively easy if the design contraints were limited to simply providing well-regulated voltages, but power supply requirements are typically much more complicated. For example, multiple power rails must be sequenced and/or track each other to ensure proper system behavior. High power sections of the design are often powered down when not in use, requiring multiple shutdown options. Powering analog circuitry adds the demand for clean, low noise supplies—no switching transients or excessive voltage ripple allowed. And, of course, all supplies must be generated as efficiently as possible to minimize power consumption.

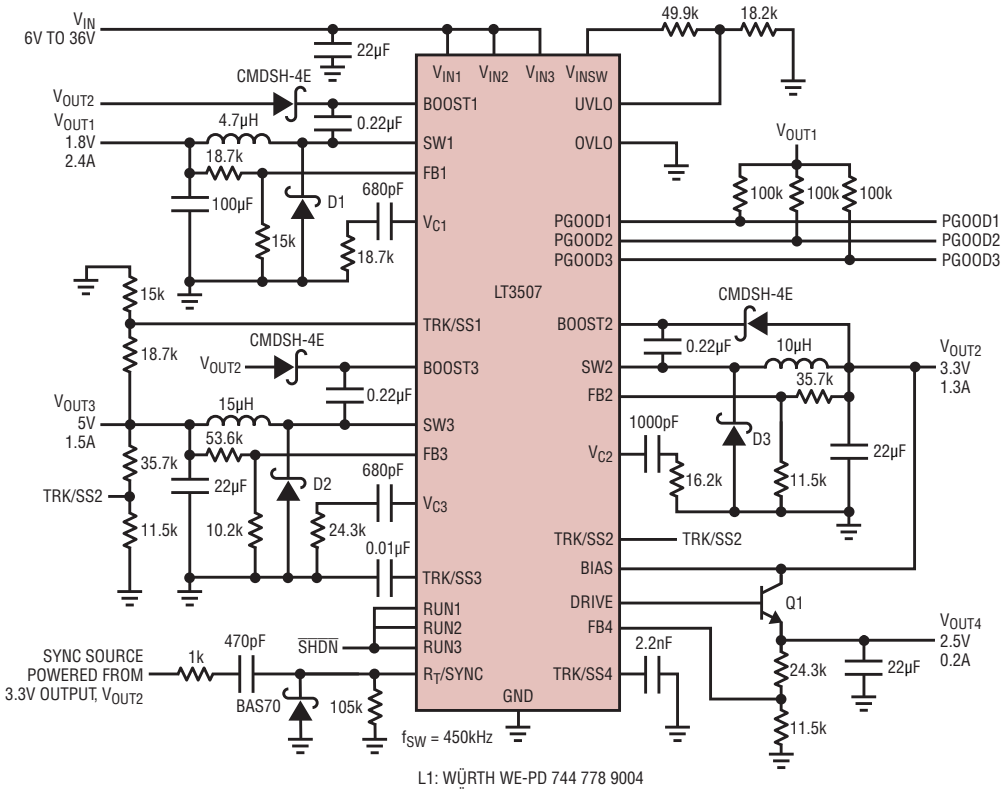
The LT3507 meets these requirements by combining three switching regulators and a low dropout linear regulator in a compact 5mm × 7mm QFN package. The switching regulators have internal power switches, independent input supplies, run and track/soft-start controls, and power good indicators. The LDO requires an external NPN pass transistor and includes track/soft-start control.

Three Independent Switching Regulators...

The LT3507 includes three independent, monolithic switching regulators to achieve a space saving solution. Channel 1 is capable of providing up to 2.4A of output current. Channels 2 and 3 are each capable of providing up to 1.6A of output current. Each of the three switching regulators has its own input supply pin to the power switch. The regulators may be operated from different supplies in order to maximize system efficiency.

The maximum voltage on any of the V_{IN} pins is 36V. The LT3507 internal circuitry is powered from V_{IN1}, which requires a minimum operating voltage for V_{IN1} of 4V. The minimum operating voltage for V_{IN2} and V_{IN3} is 3V. Since V_{IN1} powers the internal circuitry, it must always be at least 4V when any channel is running, even if Channel 1 is off.

All three regulators use a current mode, constant frequency



L1: WÜRTH WE-PD 744 778 9004
L2: WÜRTH WE-PD 744 778 9115
L3: WÜRTH WE-PD 744 778 910
D1, D2, D3: DIODES, INC. B240A
Q1: ON SEMICONDUCTOR NSS30101LT1G

Figure 1. The LT3507 in a wide input range, quad output application

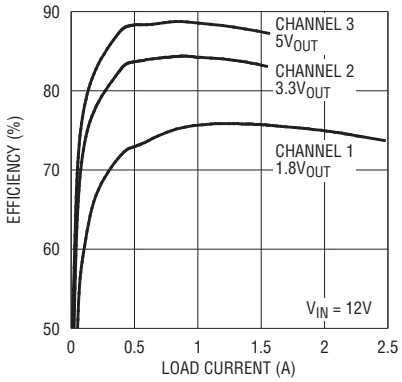


Figure 2. Switching regulator efficiency

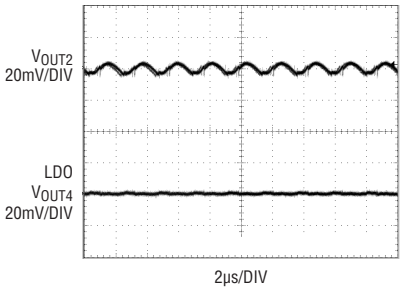


Figure 3. The LT3507's built-in LDO offers a low noise output

architecture, which simplifies loop compensation. External compensation allows custom tailoring of loop bandwidth, transient response and phase margin. The feedback reference is 0.8V, allowing output voltages as low as 0.8V.

The regulators share a master oscillator that is resistor programmable from 250kHz to 2.5MHz, or can be synchronized to an external frequency in the same range. Each regulator features frequency foldback in overload conditions to improve short circuit tolerance. Channel 1 operates 180° out of phase with respect to channels 2 and 3 to reduce input current ripple.

...and a Low Dropout Linear Regulator

The LT3507 also includes an LDO linear regulator that uses an external NPN pass transistor to provide up to 0.5A of output current. The base drive can supply up to 10mA of base current to the pass transistor and is current limited. The LDO is internally compensated and is stable with output capacitance of 2.2µF or greater. It uses the same 0.8V feedback reference as the switching regulators.

The LDO drive current is drawn from the BIAS pin if it's at least 1.5V higher than the DRIVE pin voltage, otherwise it's drawn from V_{IN1}. This reduces the power consumption of the LDO, especially when V_{IN1} is at high voltages.

The LDO does not have a separate RUN pin; it is powered up when any of the RUN pins are high. The LDO can be shut down when it is not used by pulling the FB pin above 1.25V with at least 30µA. If independent control of the LDO is needed, the LDO output can be forced to 0V by pulling the TRK/SS4 pin low. If the track or soft-start functions are needed, use an open drain output in parallel with the track or soft-start circuitry described below. If track and soft-start are not necessary, then a standard CMOS output (from 1.8V to 5V) is sufficient.

Run Control

Each of the switching regulators has a RUN pin to allow flexibility in shutting off power domains. The RUN pin is a wide range logic input and can be driven from 1.8V CMOS logic, directly from V_{IN} (up to 36V), or anywhere in between. The RUN pin draws a small amount of current to bring the reference up. This current is about 3µA at 1.8V and 40µA at 36V. The RUN pin should be pulled low (not left floating) when the regulator is to be shut down. When all three RUN pins are pulled low, the LT3507 goes into a low power shut down state and draws less than 1µA from the input supply.

The LT3507 includes three independent, monolithic switching regulators to achieve a space saving solution. Each of the three switching regulators has its own input supply pin to the power switch. The regulators may be operated from different supplies in order to maximize system efficiency.

Track/Soft-Start Control

Each regulator and the LDO has its own track/soft-start (TRK/SS) pin. When this pin is below the 0.8V reference, the regulator forces its feedback pin to the TRK/SS pin voltage rather than to the reference voltage. The TRK/SS pin has a 1.25µA pull-up current source. The soft-start function requires a capacitor from the TRK/SS pin to ground. At start-up, this capacitor is at 0V, which forces the regulator outputs to 0V. The current source slowly charges the capacitor voltage up and the regulator outputs ramp up proportionally. Once the capacitor voltage reaches 0.8V, the regulator locks onto the internal reference instead of the TRK/SS voltage.

The tracking function is achieved by connecting the slave regulator's TRK/SS pin to a resistor divider from the master regulator output. The master regulator uses a normal soft-start capacitor as described above to generate the start-up ramp that controls the other regulators. The resistor divider ratio sets the type of tracking, either coincident (ratio equal to slave feedback divider ratio) or ratiometric (ratio equal to master feedback divider ratio plus a small offset).

Undervoltage and Overvoltage Protection

Each switching regulator has its own input undervoltage shutdown to prevent the circuit from operating erratically in undervoltage conditions. V_{IN1} shuts down at 4.0V, and because it's the primary input voltage, it turns off the entire LT3507. V_{IN2} and V_{IN3} shut off at 3.0V and only shut off the switch on the affected channel.

The LT3507 also has a user programmable undervoltage and overvoltage lockout. The undervoltage lockout can protect against pulse stretching and regulator dropout. It can also protect the input source from excessive current since the buck regulator is a constant power load and draws more current when the input source is low. The overvoltage lockout

can protect the rectifier diodes from excessive reverse voltage and can prevent pulse-skipping by limiting the minimum duty cycle. Both of these lockouts shut off all four regulators when tripped.

These functions are realized with a pair of built in comparators at inputs UVLO and OVLO. A resistor divider from the VINSW pin to each comparator input sets the trip voltage and hysteresis. The VINSW pin pulls up to V_{IN1} when any RUN pin is pulled high, and is open when all three RUN pins are low. This reduces shutdown current by disconnecting the resistor dividers from the input voltage. These comparators have a 1.2V threshold and also have 10µA of hysteresis. The UVLO hysteresis is a current sink while the OVLO hysteresis is a current source. UVLO should be connected to VINSW and OVLO connected to ground if these functions aren't used.

Frequency Control

The switching frequency is set by a single resistor to the R_T/SYNC pin. The value is adjustable from 250kHz to 2.5MHz. Higher frequencies allow smaller inductors and capacitors, but efficiency is lower and the supply has a smaller allowable range of step-down ratios due to the minimum on and off time constraints.

The frequency can also be synchronized to an external clock by connecting it to the R_T/SYNC pin. The clock source must supply a clock signal whenever the LT3507 is powered up. This leads to a dilemma if the clock source is to be powered from one of the LT3507 regulators: there is no clock until the regulator comes up, but the regulator won't come up until there's a clock! This situation is easily overcome with a capacitor, a low leakage diode and a couple of resistors. The capacitor isolates the clock source from the R_T/SYNC pin until the power is up and the resistor on the R_T/SYNC pin sets the initial clock frequency. The application in Figure 1 shows how this is done.

Typical Application

Figure 1 shows a typical LT3507 application. This application allows a very wide input range, from 6V to 36V. It generates four outputs: 5V, 3.3V, 2.5V and 1.8V. Efficiencies for three of the outputs are shown in Figure 2. The LDO produces a particularly low noise output at 2.5V, as shown in Figure 3.

The outputs are set to coincident tracking using the 5V supply as the master. But wait, there's no resistor divider on the TRK/SS4 pin! It's no mistake; the LDO output coincidently tracks the supply it's sourced from (the 3.3V supply in this case) as long as Q1 is a low V_{CESAT} transistor, such as the NSS30101 used here. Just remember that this little cheat only works for coincident tracking. Figure 4 shows the start-up waveforms of the four outputs.

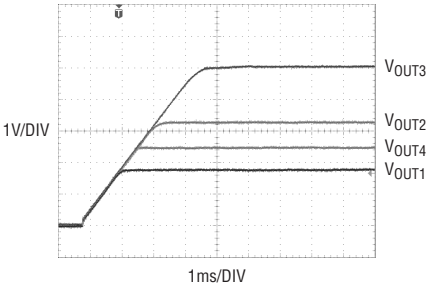


Figure 4. Coincident tracking waveforms

In this application, the clock is synchronized to an external source that is powered from the 3.3V output. A capacitor isolates the clock until the 3.3V supply is good, and then passes the clock signal to the RT/SYNC pin. It should be noted that the LDO can actually supply up to 0.5A as long as $I_{OUT4} + I_{OUT2} \leq 1.5A$.

Conclusion

The LT3507 provides a compact solution for four power supplies. Its tiny 5mm × 7mm QFN package includes three highly efficient switching regulators and a low dropout linear regulator. Just a few small inductors and ceramic capacitors are needed to create four high efficiency step-down regulators. Plenty of options insure that the LT3507 meets the needs of a wide variety of multiple output applications.

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LT5575, continued from page 13

signals as shown in Figure 6. One of these is a –48dBm CW tone, and the other is a –48dBm WCDMA carrier. These are offset in frequency so that the resulting 3rd order product appears centered about DC. Compute the intermodulation product generated in the I/Q demodulator:

- ❑ RF gain preceding LT5575: 20dB
- ❑ Signals entering LT5575: –28dBm
- ❑ LT5575 IIP3, 2-tone: 22.6dBm
- ❑ LT5575 a_3: 0.0244

A MATLAB simulation performed using a pseudo-random channel predicts distortion at LT5575 output of –135.8dBm. This result agrees well with the equation 8, which predicts a distortion power of –135.7dBm.

Refer this signal back to the receiver input:

- ❑ RF gain preceding LT5575: 20dB
- ❑ Equivalent interference level at Rx input: –155.8dBm
- ❑ Thermal noise at receiver input: –101.2dBm

The equivalent interference in this case is 54.6dB below the thermal noise at the receiver input. The resulting degradation in sensitivity is <0.1dB, so the receiver easily meets the specification of –121dBm.

Conclusion

The calculations given here using the LT5575 I/Q demodulator show that a WCDMA wide area basestation receiver can be successfully implemented using a direct conversion architecture. The high 2nd order linearity and input 1dB compression point of the LT5575 are critical to meeting the performance requirements of such a design.

Buck, Boost and LDO Regulators Combined in a 4mm × 4mm QFN

by Chris Falvey

Introduction

The LT3570 simplifies complex multi-rail power supply designs by integrating three DC/DC regulators into a single package: a current mode buck regulator, a current mode boost regulator, and an LDO controller.

The buck and boost regulators each have a current limit of 1.5A. The LDO controller has an output current capability of 10mA and combines with an external NPN transistor to create a linear regulator. The frequency of the switching regulators can be set from 500kHz to 3MHz by an external resistor or synchronized to an external oscillator. The independent input voltages for each regulator offers a wide operating range from 2.5V up to 40V. Each regulator also has its own shutdown circuitry and the buck and boost regulators have their own soft-start circuitry.

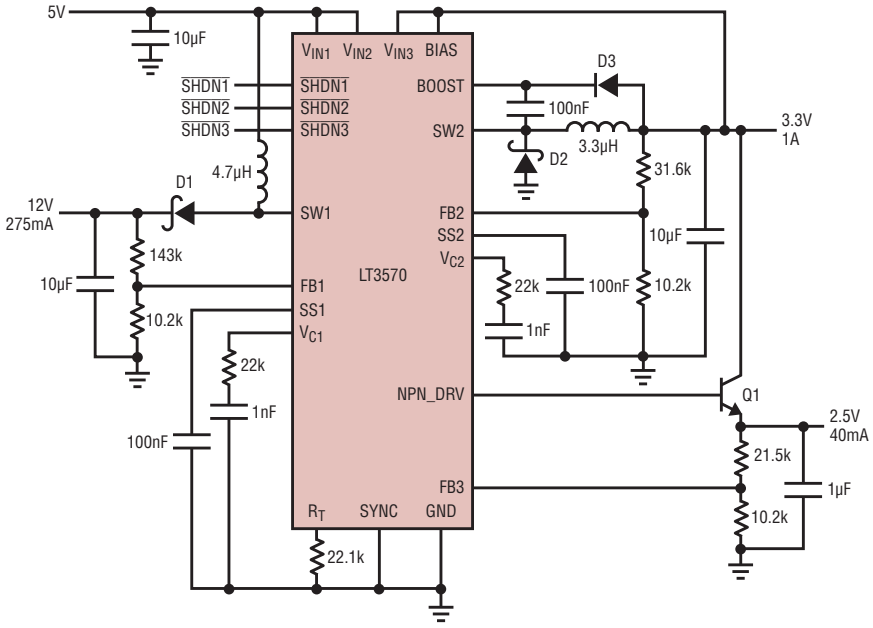
The typical application shown in Figure 1 generates 3.3V at 1A from the buck regulator, 2.5V at 40mA from the LDO controller and 12V at 275mA from the boost regulator, all from a 5V input supply voltage and with an overall efficiency around 85%.

The LT3570 simplifies complex multi-rail power supply designs by integrating three DC/DC regulators into a single package: a current mode buck regulator, a current mode boost regulator, and an LDO controller.

Features

Available in either a 24-lead 4mm × 4mm QFN or a 20-pin TSSOP package, the LT3570 is a constant frequency current mode regulator. If all $\overline{SHDN}$ pins are held low, zero quiescent current is drawn from the input supplies and the part is turned off. Any $\overline{SHDN}$ pin voltage exceeding 1.5V will turn on the corresponding regulator. A precise shutdown pin threshold allows for easy integration of input supply undervoltage lockout. All three regulators share the same internal 800mV reference voltage. For each regulator, an external resistor divider programs the output voltage to any value above the part's reference voltage. The switching frequency is set with an external resistor from the R_T pin to GND. This allows a trade off between minimizing component size (by using higher switching frequencies) and maximizing efficiency (by using lower switching frequencies). Additionally, running at a low switching frequency allows for applications that require larger V_{IN}-to-V_{OUT} ratios. The adjustable and synchronizable switching frequency also allows the user to keep the switching noise out of critical wireless and audio bands.

Both the buck and boost regulators control the slew rate of the output



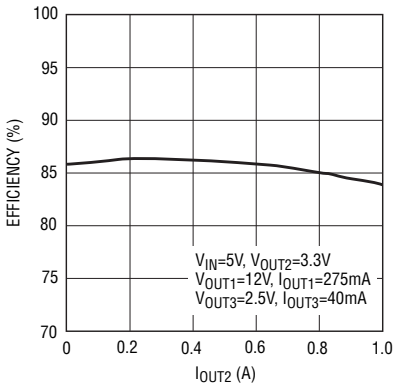


Figure 1. A typical 5V input to 3.3V, 2.5V and 12V application

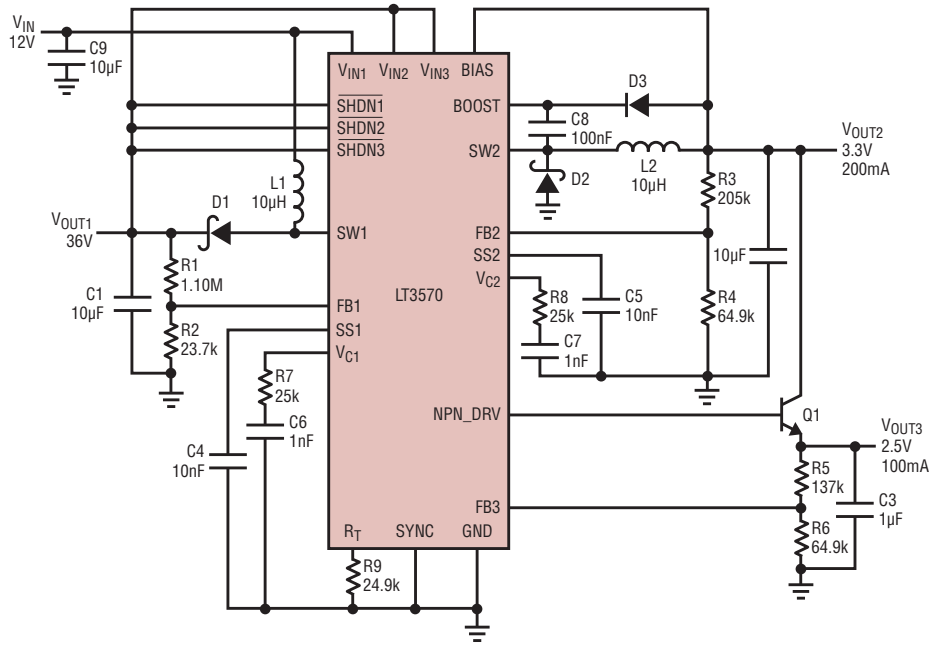


Figure 2. Dying gasp system keeps power even when battery is disconnected.

voltage during start-up. A controlled ramp reduces inrush current on the input supply and minimizes output overshoot. An external capacitor connected between the SS pin and ground programs the slew rate. The voltage on the SS pin overrides the internal reference voltage to the error amplifier and is charged by a 4.5µA internal current source.

The BIAS pin allows the internal circuitry to draw current from a lower voltage supply than the input, reducing power dissipation and increasing efficiency. Normally, the quiescent current is supplied from V_{IN2}, but when the voltage on the BIAS pin exceeds 2.5V the current is supplied from the BIAS pin. The BIAS pin is only available on the 24-lead QFN package.

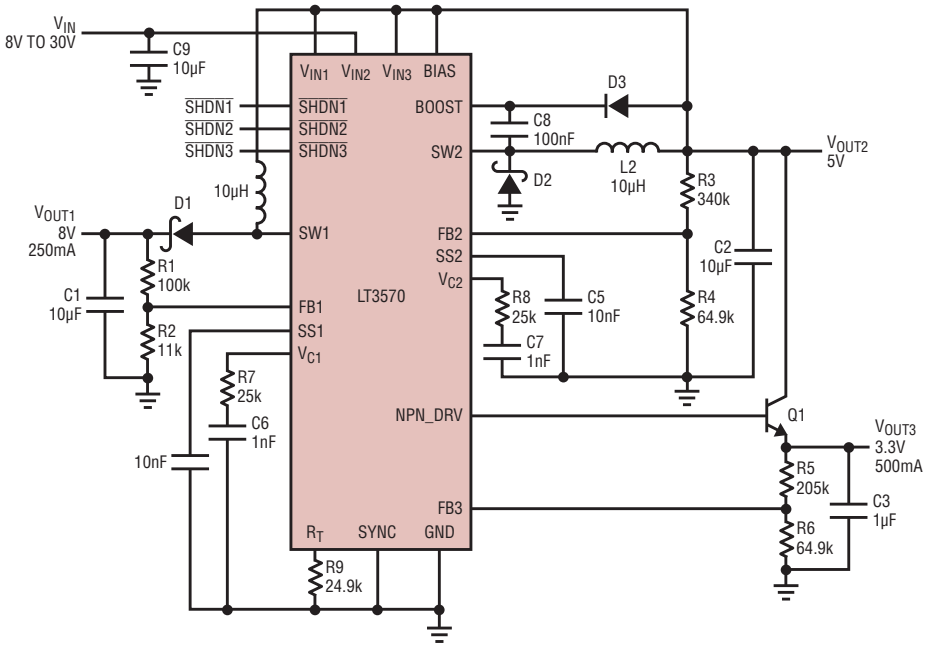


Figure 4. DSL modem application

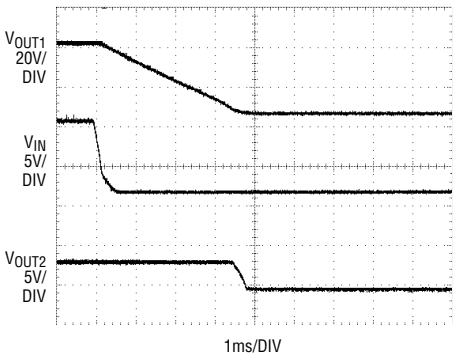


Figure 3. Output waveforms when power is removed from the circuit in Figure 2

Applications

"Dying Gasp" Application

The LT3570 provides an ideal solution for any "dying gasp" system. Figure 2 shows a typical application powering an airbag controller. In an automobile accident, the battery may get disconnected from the shock sensors yet the airbag must still fire. In this application, the battery supplies power to the boost regulator. V_{OUT1} is set to 36V and drives V_{IN2} and V_{IN3}, the inputs to the buck regulator and the LDO controller, respectively. Even after the input supply is removed, the buck regulator and the LDO continue to function properly for more than 3ms, as the energy continues to be supplied from the output capacitor of the boost regulator. The buck regulator turns off when V_{IN2} approaches the input undervoltage lockout of 2.3V (see Figure 3). *continued on page 41*

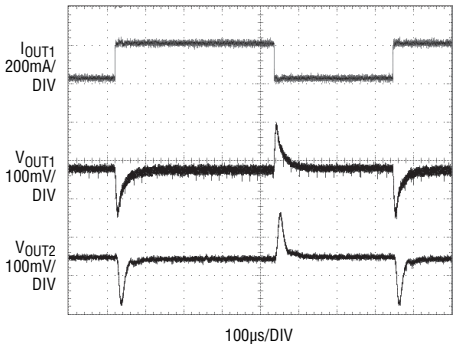


Figure 5. Step response of Figure 4 with boost current stepped from 200mA to 400mA

Compact Power Solution Overcomes Peak Power Limitations in PCMCIA-Based Pulsed-Load GSM and GPRS Applications

by Timothy Sourdif

Introduction

In an increasingly wireless world, mobile computing applications are driving the need for web-anywhere enabled notebook computers. PC Card or PCMCIA slot powered GSM/GPRS modems are now the standard for these applications. During GSM transmission peak currents can exceed 2A, well beyond the maximum current capability of the PCMCIA slot. Therefore, the modem must be designed to limit input power and draw on card-based storage for most of the energy required during a transmission cycle.

The LTC3125 is a synchronous step-up DC/DC converter that charges a reservoir capacitor up to the regulated output voltage while directly and accurately controlling the average input current. The LTC3125's 91% efficiency provides the maximum possible output current to the load without impacting the host. Together with an external bulk or reservoir capacitor, the LTC3125 can interface the GSM/GPRS modem directly to a PCMCIA power bus without overloading it.

Power Demands

Much of the work in GSM/GPRS power supply design revolves around the transmission cycle due to the high current consumption in this mode. Typically the transmitter's supply current is modulated to 2A pulses, which occupy one or more of the 577µs timeslots from the eight timeslots available.

During a GSM transmission, one timeslot is used for data transmission, the other seven are idle, during which the supply current is reduced to less than 100mA. Therefore, the average current consumed over the 4.6ms window is about 340mA. In the end, the transmitter power supply

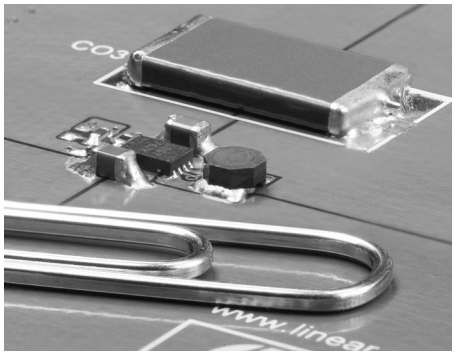


Figure 1. A complete PCMCIA-powered, low profile solution for GSM transmitters

design must be capable of an average current of 340mA but also be able to handle the 2A transmit burst currents. Higher data rate standards are also popular. For instance, the GPRS Class 10 standard allows for transmission in two of the eight available timeslots for an average current consumption of almost 575mA and 2A burst duration of 1.15ms.

Based on the standard PC card bus power (3.0V to 3.6V) specification, the maximum peak current must not exceed 1A. This is clearly not sufficient for powering these GSM/GPRS applications directly.

The Solution

The LTC3125 is a 91% efficient step-up DC/DC converter in a 2mm ×

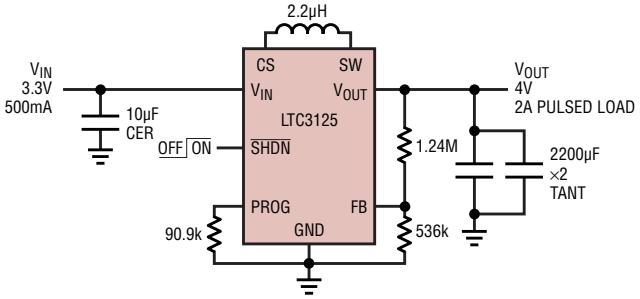


Figure 2. PC Card or CompactFlash (3.3V/500mA max) 4.0V output, GSM pulsed load

3mm × 0.75mm DFN package. The 1.5MHz switching frequency provides a compact and low profile design solution for pulsed load applications (Figure 1). The high accuracy (±5%) of the programmable input current limit allows the designer to efficiently use the maximum available source current. To accommodate a variety of card standards, the input current limit can be set to any value from 200mA to 1A by an external programming resistor. Output disconnect ensures that the output is completely discharged in shutdown. The LTC3125 also eliminates inrush current during start-up, maintaining control of the current seen by the input supply when low ESR reservoir capacitors are being charged. Additional features include antiringing control for EMI suppression, short-circuit protection, automatic Burst Mode operation, soft-start and thermal overload protection.

Recent developments in ultra- or super-capacitors as well as high value tantalum capacitors have vastly increased the available capacitance for a given volume while achieving very low ESR. Low profile bulk output capacitors are available to supply the energy to the load and maintain the output voltage within the specified limits during the high current pulses. High capacitance and low ESR can lead to instability in typical internally compensated step-up DC/DC converters. The internal loop compensation of the LTC3125 is optimized for use with any output capacitor value greater than 500µF. Figure 2 shows the LTC3125 powered from a standard 3.3V/500mA PC card port. The 500mA input current limit is set by R_X. Here, two 2200µF, low profile, Vishay TANTAMOUNT solid tantalum capacitors provide power to the load during pulsed load events. Given the magnitude and the duration of the pulsed load current, the capacitors are chosen to meet the output voltage droop specification, typically 300mV. Neglecting the input current supplied by the source, the total output voltage droop is given by:

$$V_{DROOP} = I_{PULSE}\left(R_{ESR} + \frac{t_{PULSE}}{C_{OUT}}\right)$$

Where V_{DROOP} is the change in output voltage, I_{PULSE} and t_{PULSE} are the peak pulse current and duration respectively, R_{ESR} is the capacitor ESR and C_{OUT} is the output capacitance.

During and after the load pulse the LTC3125 will draw the maximum input current set by Rprog to charge the reservoir cap until the desired terminal output voltage is reached.

During GSM transmission peak currents can exceed 2A, well beyond the maximum current capability of the PCMCIA slot. Therefore, a PCMCIA-based modem must be designed to limit input power and draw on card-based storage for most of the energy required during a transmission cycle.

If the load pulse is periodic, as in the GSM application, it is desirable to insure that the capacitor recharges during the idle timeslots. The time to re-charge the reservoir capacitor(s) is approximately:

$$t_{RECHARGE} = \frac{C_{OUT} \bullet V_{DROOP} \bullet V_{OUT}}{\eta \bullet I_{INPUT} \bullet V_{IN}}$$

Where $t_{RECHARGE}$ is the time for the LTC3125 to raise the output voltage back to its terminal value, C_{OUT} is the output capacitance, V_{OUT} is the average terminal output voltage, V_{DROOP} is the previously calculated droop, η is the fractional converter efficiency (η = 1 is 100% efficiency), V_{IN} is the input voltage and I_{INPUT} is the input current limit.

Both of these factors, voltage droop and re-charge time, ultimately determine the required reservoir capacitor size. The typical pulsed load response for the circuit in Figure 2 is shown in Figure 3.

Charging High Density Capacitors

Larger supercapacitors are commonly used in hold-up power sources where they deliver power in the event of a main power source failure or removal. The LTC3125's input current limit, soft start feature and its ability to operate with input voltages exceeding the output voltage, make it an ideal converter to safely regulate the voltage across the large output capacitors while still protecting the input power supply. The LTC3125 step-up converter maintains voltage regulation even when the input voltage is above the desired output voltage. Figure 4 shows the response of the LTC3125 charging a 15F, 2.5V super capacitor.

Conclusion

The compact LTC3125 step-up DC-DC converter with ±5% accurate, programmable average input current limit is an optimal GSM/GPRS power supply solution for PCMCIA/PC Card slot powered peripherals. Its high efficiency combined with today's low profile supercapacitors elegantly solves the pulsed load problem with a compact solution footprint.

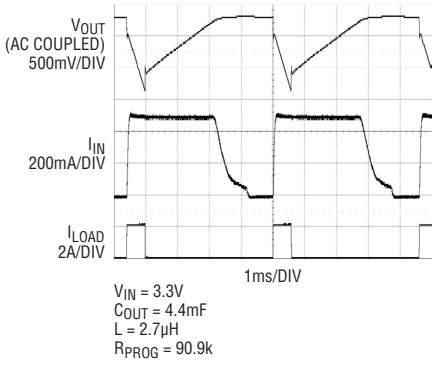


Figure 3. Waveforms of input current and V_{OUT} for a pulsed load current

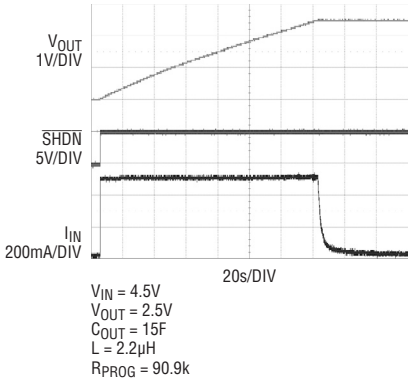


Figure 4. Waveforms of input current and V_{OUT}, charging large C_{OUT} from 0 volts

Multi-Rail DC/DC Converter in a 3mm × 3mm QFN Takes Inputs as Low as 0.7V

by Dave Salerno

Introduction

Modern handheld instrumentation, portable medical devices and consumer electronics demand a multitude of power rails for internal processors, memory, audio and color displays. Popular battery technologies for these devices include single or multiple cell alkaline, NiMH or Li-Poly/Li-Ion batteries. Operation from a USB port or a wall adapter is another common trait. Replaceable alkaline batteries are particularly attractive for remote locations and portable medical devices where power or time is not available to recharge batteries. The challenge is to create a compact and efficient power solution for these wide V_{IN} range, multi-output applications. The LTC3100 multichannel DC/DC converter makes it easier to meet this challenge.

The LTC3100 is a high efficiency, 1.5MHz multichannel DC/DC converter in a compact 3mm × 3mm × 0.75mm QFN package. It features a synchronous step-up (boost) DC/DC converter, a synchronous step-down (buck) DC/DC converter and a 100mA low dropout linear regulator (LDO).

The boost and buck converters can operate independently from different sources, from the same source, or cascaded to create a buck-boost converter. Internal loop compensation simplifies the design and minimizes external component count and solution size. Each converter has a Power Good indicator that is useful for voltage sequencing. The boost converter offers up to 95% efficiency and features true output disconnect, a 700mA minimum current limit and can start with input voltages as low as 700mV, making it ideal for single alkaline or NiMH cell applications. The buck converter offers up to 94% efficiency and can deliver 250mA or more from input voltages between 1.8V and 5.25V. Both converters feature automatic Burst Mode® operation for high efficiency at light loads. For low noise applications, Burst Mode operation can be disabled by grounding the MODE pin. The 100mA LDO, whose input is internally connected to the boost output, can be used to produce a third, low noise output. It can also be used for voltage sequencing of the boost output voltage.

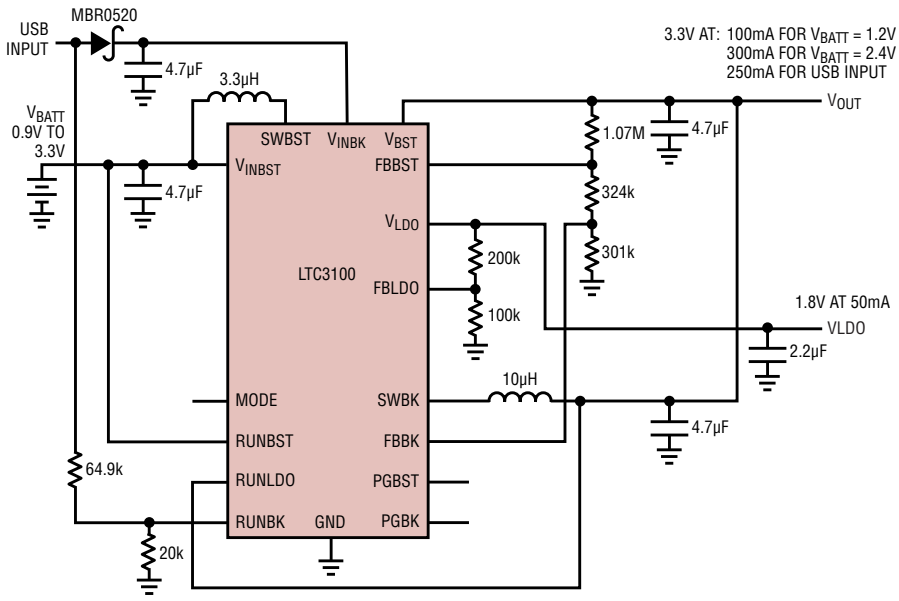


Figure 1. Multiple-input source 3.3V and 1.8V converter

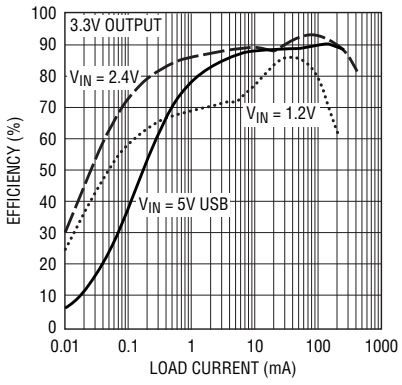


Figure 2. Converter efficiency for the circuit of Figure 1

The circuit shown in Figure 1 takes advantage of the LTC3100's ability to operate from independent input sources to generate multiple outputs regardless of which power source is available. In this example, the boost converter produces a regulated 3.3V output from a single- or dual-cell input voltage. The buck converter runs from a 5V USB or wall adapter input and produces 3.3V as well, with its output externally tied to that of the boost.

By leaving the MODE pin open, the automatic Burst Mode operation feature of the LTC3100 is enabled, maximizing battery life at light load. When USB or wall adapter power is available, the buck converter is automatically enabled and generates a 3.3V output that is set 3.8% higher than that of the boost converter. This puts the boost converter in sleep mode, reducing the load on the batteries to just a few micro-amps. The result is a 3.3V output that seamlessly transitions from battery power to USB

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Dual ADC Driver with Tightly Matched Gain and Phase Raises Quadrature Demodulation Performance

by Kris Lokere

Introduction

High speed differential amplifiers help to drive high performance analog-to-digital converters (ADCs) by providing balanced drive to the differential input stage, setting the common mode level, absorbing the sampling-energy, and taking gain to reduce the output swing requirement of preceding circuitry. In applications involving multiple ADCs, a compact, tightly matched dual differential amplifier such as the LTC6420-20 can further simplify the design by reducing the uncertainty of channel-to-channel variations.

The LTC6420-20 features two 1.8GHz differential amplifiers, each capable of driving 12-, 14- and 16-bit pipeline ADCs at low noise and low distortion levels, even for input frequencies as high as 300MHz. The internal op amps are manufactured on a Silicon Germanium (SiGe) process and feature an ultra-low 1nV/$\sqrt{\text{Hz}}$ noise density. Even after factoring in the internal feedback resistors, the total input noise density equals only 2.2nV/$\sqrt{\text{Hz}}$. The channel-to-channel gain matching is production tested and guaranteed to be better than ±0.25dB. Moreover, the monolithic design ensures that both phase and group delay remain tighly matched over the entire bandwidth of the amplifiers.

In applications involving multiple ADCs, a compact, tightly matched dual differential amplifier simplifies design by reducing the uncertainty of channel-to-channel variations.

The dual amplifier is available in a 3mm × 4mm QFN package, which saves space compared to two single amplifiers. For further space-savings, all gain and feedback resistors are included on-chip, setting a fixed voltage gain of 20dB. The LTC6420-20 consumes 80mA per channel from a supply as low as 2.85V. A 40mA version, the LTC6421-20, is available to save power at the expense of usable input bandwidth.

Wideband Interface Between an I/Q Demodulator and a Dual ADC

When an IF or RF signal is applied to a demodulator such as the LT5575, the signal's information is separated out into two baseband signals: "in-phase" (I) and "quadrature" (Q). Both baseband signals need to be digitized simultaneously, and it is critical that the relationship of gain and phase between the two is maintained. Furthermore, if you want to maximize the dynamic range by driving the dual

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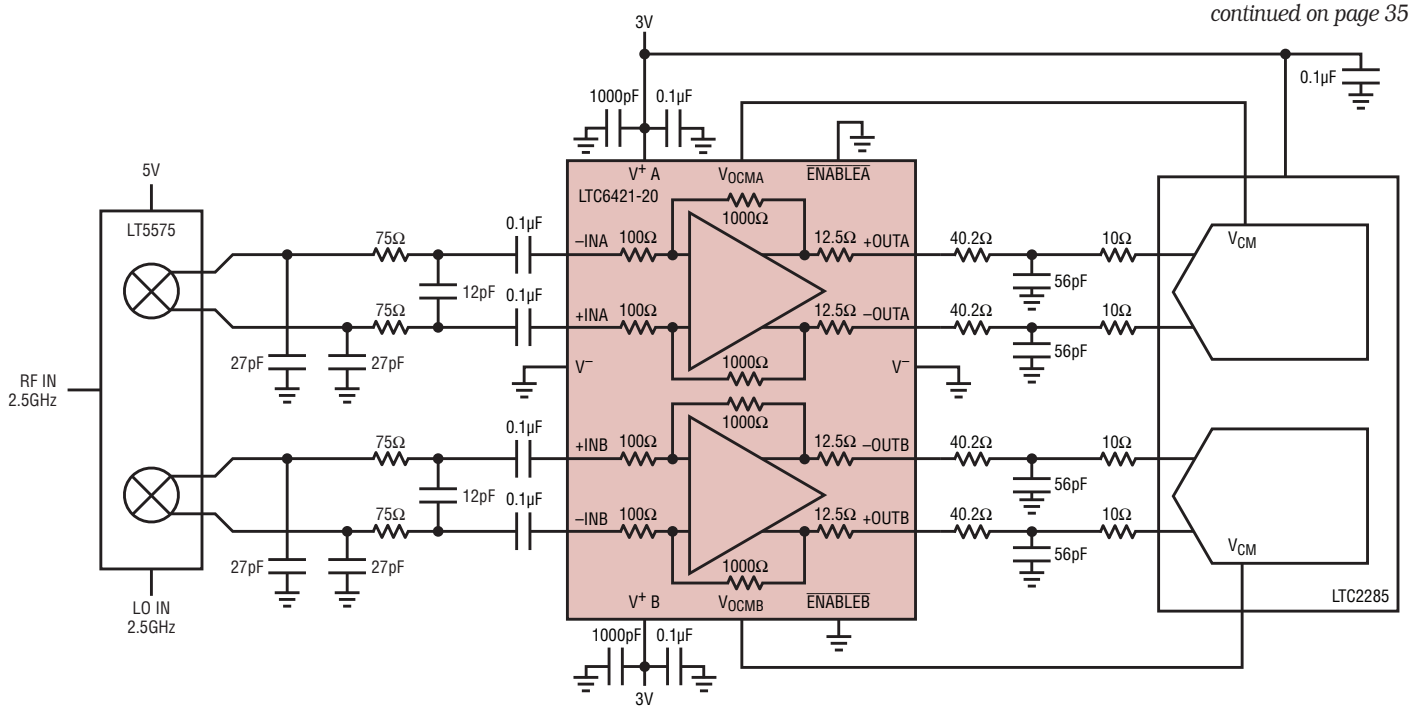


Figure 1. The voltage gain of the LTC6421-20 reduces the output swing requirements of the LT5575 demodulator. This improves overall system linearity.

No PWM Signal Needed for Accurate Dim/Bright Control of Automotive Brake Lights and Other Signal LEDs

by Bill Martin

Introduction

LEDs are quickly becoming standard lighting for a variety of commercial, automotive, and industrial applications. Some of these applications require wide-range brightness control, spurring a demand for products that offer PWM-based LED brightness control. However, many applications only require two settings, bright and dim, so generating a PWM signal for a binary choice is inconvenient overkill. The LT3592 LED driver is the solution to this problem. It simplifies design by offering two LED current settings with a 10:1 ratio, selected via a simple digital control pin. This pin has a low threshold voltage, but high voltage capability, making it very easy to plug into any automotive or industrial system. For an application such as automotive brake light control, the LT3592's accurate, consistent output current levels and easy to use small package make it a perfect fit. Furthermore, the LT3592 is rugged enough to tolerate a 36V maximum input, making it useful in a wide variety of higher voltage applications.

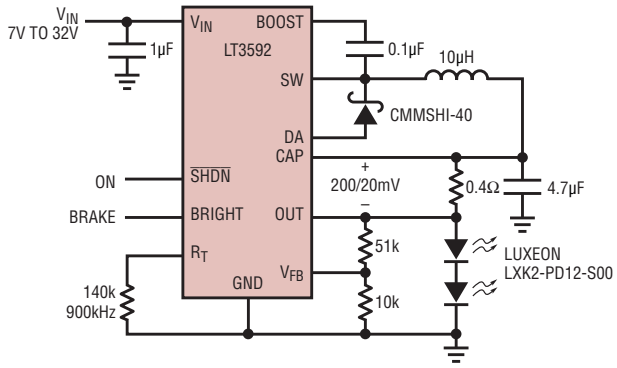


Figure 1. Two red LED application with no external boost diode

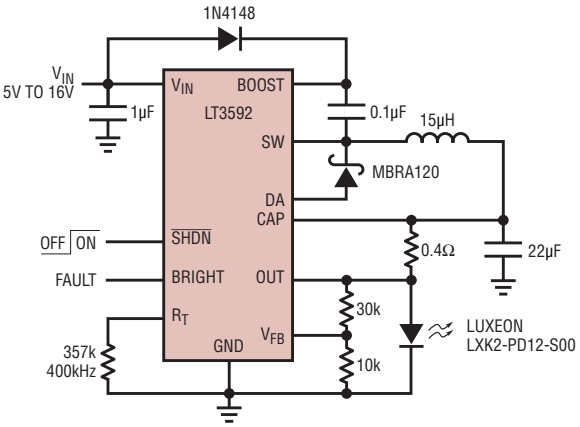


Figure 2. Single red LED application with external boost diode to V_{IN}

Simple 2-Level Current Control

The LT3592 uses a single external current sense resistor between the CAP and OUT pins to set its two output current levels, which have a 10:1 ratio. In bright mode, an internal amplifier regulates the voltage difference between CAP and OUT to 200mV. In dim mode, the voltage is regulated to 20mV. Using a 0.4Ω current sense resistor results in a bright current of 500mA and a DIM current of 50mA. Switching between the high and low current levels couldn't be easier—bring the BRIGHT pin above 1.4V for high current, and below 0.3V for low current. The bright current level can be as high as 500mA.

The output voltage of the LT3592 can be as high as 20V, but the part is also designed to work well with single red LEDs, which can have forward voltages below 2V at reasonable current levels. The operating frequency can be set anywhere between 400kHz and 2.2MHz using a single resistor from the RT pin to ground. Set a lower operating frequency for the best efficiency, and a higher frequency for smaller filter components and overall solution size. The LT3592 also incorporates an

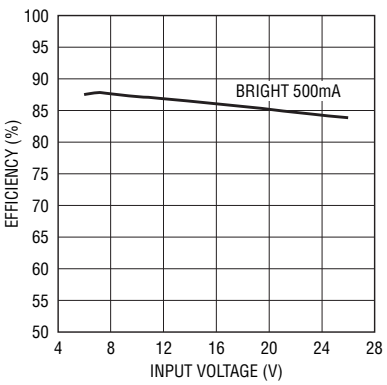


Figure 3. Efficiency for Figure 1

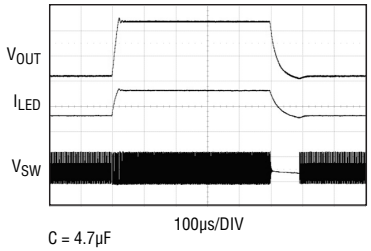


Figure 4. Switching between dim (50mA) and bright (500mA) modes with 4.7µF output cap

internal Schottky diode between CAP and BOOST, which saves an external component for applications with two or more series LEDs (see Figure 2 for a single LED solution).

Rugged Solution for Tough Environments

In addition to an internal switch current limit circuit, the LT3592 includes a catch diode current sense limit function that protects the circuit during start-up at high input voltages. Simply connect the anode of the Schottky catch diode to the DA pin, and the LT3592 automatically reduces the oscillator frequency when the catch diode current is higher than 1A. The lower operating frequency prevents the inductor current from ramping up in an uncontrolled fashion and allows the switch current limit to be effective by avoiding minimum on time restrictions. The LT3592 also automatically reduces its operating frequency if the LED string shorts out, minimizing power dissipation in the part.

The $\overline{\text{SHDN}}$ and BRIGHT pins are as rugged as the V_{IN} pin and can withstand up to 36V, so they can be tied to the input voltage. Nevertheless, both pins have low voltage thresholds that allow them to be directly interfaced to low voltage microcontrollers.

The LT3592 is not only useful for LED applications. It has a fully functional voltage control loop, and the current loop can be used as an accurate current clamp for voltage output applications. The voltage loop is also useful as a voltage clamp in case of an open LED fault. The transition between voltage and current control is stable and seamless.

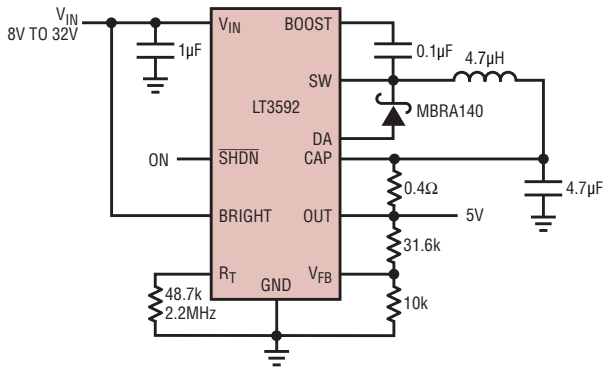


Figure 5. A 5V power supply with a 500mA current limit

Conclusion

The LT3592 makes 2-state bright/dim LED control simple and rugged. It is an ideal solution for applications such as automotive brake lights and flashing warning lights in industrial systems. Accurate control of the current levels makes LED brightness consistent across units in a given application regardless of varying LED forward voltage characteristics. Switching between the two current levels can be accomplished with either very low or very high voltage level digital signals.

LTC6420, continued from page 33

ADC close to full scale, without driving the demodulator so hard that it causes excessive distortion, you need to insert some gain between the demodulator output and the ADC input. In Figure 1, the LTC6421-20 provides this gain, while the tight matching between its two channels contributes a negligible amount of gain or phase error. The bandwidth and linearity of the LTC6421-20 ensures that 14-bit linearity (distortion less than –84dBc) is maintained to 50MHz and beyond, an important design criteria in digital-predistortion (DPD) circuits or wideband receivers.

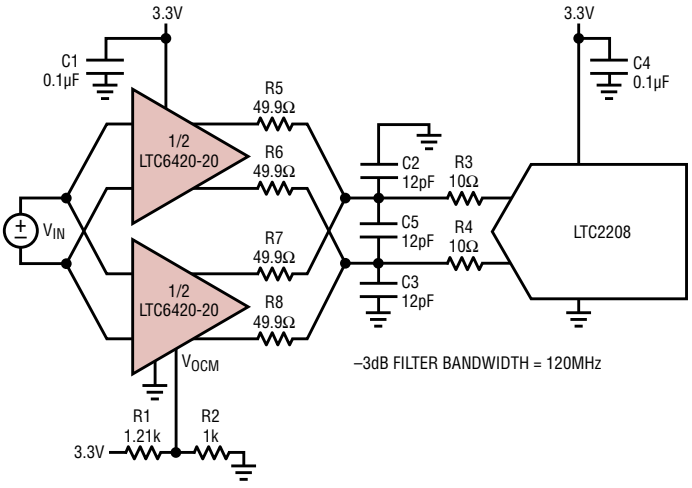


Figure 2. Connecting the two channels of the LTC6420-20 in parallel reduces the noise floor

Paralleling Two Drivers to Lower the Noise Floor

In applications with only one ADC, you can hook-up the two channels of the dual amplifier in parallel, as shown in Figure 2. The main benefit of doing so is a reduction in noise, because the random noise contributions of each channel get averaged out. For example, input noise density (with inputs shorted) drops from $2.2nV/\sqrt{Hz}$ to $1.5nV/\sqrt{Hz}$, a 3dB improvement in SNR if the driver were the dominant noise source.

Conclusion

The LTC6420 features two high speed differential amplifiers in a small 3mm × 4mm QFN package, with guaranteed tight matching specs between the two channels. It is ideal for driving high frequency signals into dual ADCs, especially when board space is limited or when the magnitude and phase relationship between the signals must be preserved.

White LED Driver with Output Disconnect and 1-Wire Current Programming

by Ahmed Hashim

Introduction

The LT3593 is designed to drive up to ten white LEDs in series from a single lithium-ion cell, ensuring matched LED current and eliminating the need for ballast resistors. The LT3593 internally compensated step-up DC/DC converter switches at 1MHz so that it can be used with tiny, low profile external components.

The LT3593 features an internal 5-bit DAC, allowing the LED current to be programmed using only one pin. The device features true output disconnect in shutdown as well as a unique high side current sense allowing it to function as a "1-wire" current source where the low side of the LEDs can be returned to ground anywhere. A typical application schematic along with expected efficiency can be seen in Figure 1. The functionality and feature set available in the LT3593 make it ideal for portable electronics display back-lighting applications. The LT3593 is available in a 6-lead (2mm × 2mm) DFN as well as 6-lead SOT-23.

1-Wire Current Programming

The LED current can be programmed linearly to 32 unique values by strobing the CTRL pin. A 5-bit internal counter is decremented on each rising edge on the CTRL pin, reducing the programmed current by 625µA from the full-scale current of 20mA with each step. The programmed LED current can be calculated using the following equation:

$$I_{LED} = 20mA - (N - 1) \bullet 625\mu A$$

where N is the number of rising edges on the CTRL pin. Strobing the CTRL pin more than 32 times results in the minimum current of 625µA. The CTRL pin must stay high after the last CTRL strobe and 128µs later the part will turn on and start to regulate the programmed current. To shut down the part, the CTRL pin is held low; 128µs after the falling edge of CTRL, the part shuts down. Figure 2 shows current programming and shutdown timing.

If the LED current needs to be reprogrammed, there is no need to shutdown and then reprogram. The LT3593 can be reprogrammed from one LED current to another by simply strobing the CTRL pin and, 128µs after the last rising edge, the part starts regulating the newly programmed current (also shown in Figure 2).

Buck-Boost Mode

If a low number of LEDs is needed, there could be a case where the required output voltage is lower than the input voltage. In this case, the LT3593 can be used in buck-boost mode where the LED string is returned to the input supply instead of ground. Figure 3

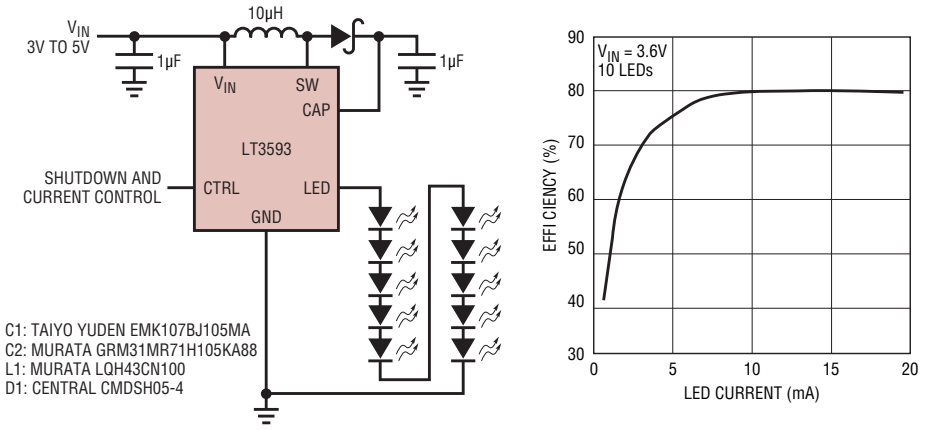


Figure 1. LED driver for ten white LEDs

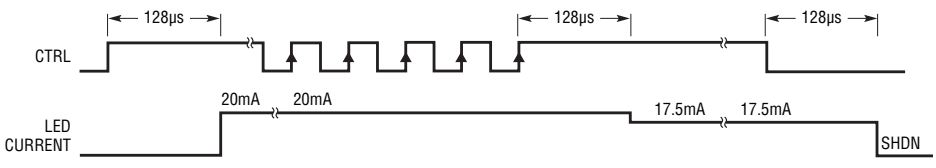


Figure 2. Current programming and shutdown timing

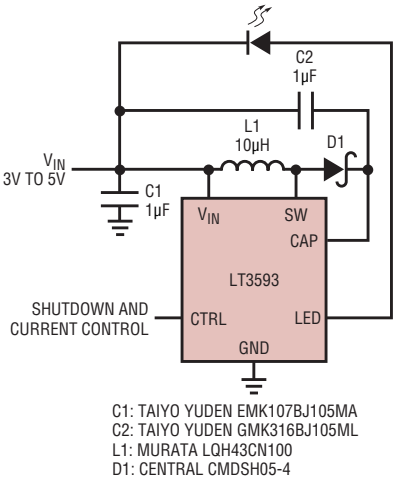


Figure 3. LED driver in Buck-Boost mode driving one LED

shows an application where a single LED is driven from a 5V supply.

Output Disconnect

The LT3593 has an internal disconnect switch that is used to sense the LED current during normal operation. This internal switch also serves to provide output disconnect during shutdown so that the LEDs are truly disconnected from the output of the regulator.

Fault Protection

The LT3593 protects against both open and shorted LED faults. In the case of an open LED fault, the output voltage V_{CAP} continues to rise. Once V_{CAP} reaches 38V, an open fault is triggered and the part goes into a low frequency mode clamping the output to 38V and minimizing input current. A waveform showing the LT3593's response to an open LED fault can be seen in Figure 4.

In a shorted LED fault, the LED pin can be shorted to ground, running excessive current from V_{CAP}. To protect from such a fault, the LT3593 limits the maximum current out of the LED pin to approximately 45mA.

Conclusion

The LT3593 is a step-up LED driver that can drive up to ten white LEDs from a single lithium-ion cell. It can easily be programmed through a single pin interface and combines many desirable features as well as fault protection against open or shorted LEDs.

The feature-rich LT3593 is available in the 6-lead (2mm × 2mm) DFN as well as the 6-lead SOT-23. These two small, low profile packages, together with internal compensation and an output disconnect device, are ideal for a complete small board area LED driver solution, especially in portable device display backlighting applications.

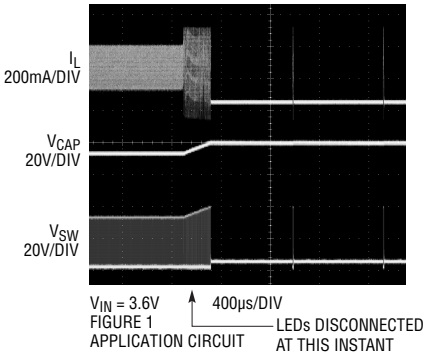


Figure 4. Open LED fault protection

LTC3100, continued from page 32

power while maximizing battery life. The diode on the USB input prevents any reverse current from the 3.3V output (while operating on batteries) back to the USB input when it is open or grounded. Figure 2 shows the converter efficiency versus load with various input sources, illustrating the high efficiency over a wide load range. The LDO in the LTC3100 (with its input internally tied to the Boost output) provides a second regulated output, in this case programmed to 1.8V.

Because the buck converter input can come from the boost output, the LTC3100 can function as an ultra-low voltage buck-boost converter, providing a regulated 1.2V output from a single alkaline or NiMH cell. This is shown in Figure 3, where the LTC3100 generates two regulated outputs from a single cell input (whose voltage may be above or below 1.2V) by boosting V_{IN} up to 3.5V and then regulating down to 1.2V and 3.3V using the buck and the LDO. In this example, the Power Good outputs and the LDO are used to provide voltage sequencing, so that the 1.2V core supply comes up before the 3.3V I/O supply, as shown in the scope photo of Figure 4. The LDO also provides additional noise filtering and ripple rejection for the 3.3V output, guaranteeing a low noise output for sensitive analog circuitry, even when the converters are in Burst Mode operation.

Conclusion

The LTC3100 is a high efficiency, multichannel converter that can operate from a wide range of voltage sources. Independent input voltages for each converter, Power Good outputs and an LDO make the LTC3100 a small, highly integrated and flexible solution for many demanding applications.

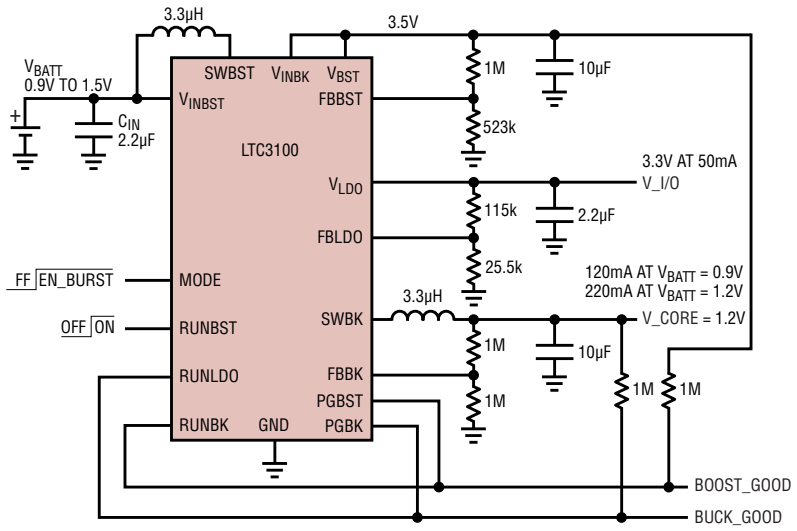


Figure 3. Single-cell dual output converter with voltage sequencing

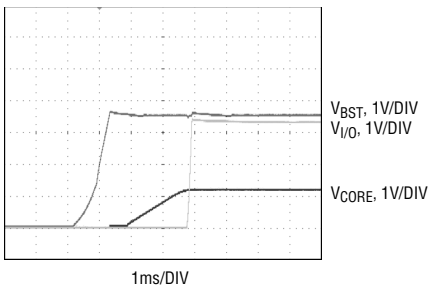


Figure 4. Voltage sequencing of the output voltages for the circuit of Figure 3

Ideal Diode Betters a Schottky by a Factor of Four in Power and Space Consumption

by Meilissa Lum

Introduction

High availability systems often use parallel power supplies or battery feeds to achieve redundancy and enhance system reliability. Traditionally, Schottky ORing diodes are used to connect these supplies at the point of load and prevent backfeeding into a faulty power supply. Unfortunately, the forward voltage drop of these diodes reduces the available supply voltage and dissipates significant power at high currents—costly heat sinks and elaborate layouts are needed to keep the diodes cool.

When power dissipation is a concern, the Schottky diode can be replaced with a MOSFET-based ideal diode. This reduces the voltage drop and power dissipation, thereby reducing the complexity, size and cost of the thermal layout and increasing system efficiency. The LTC4355, LTC4357 and LTC4358 enable MOSFET-based ideal diode solutions for various applications—the choice depends on the current and operating voltage of the application. Table 1 compares these devices.

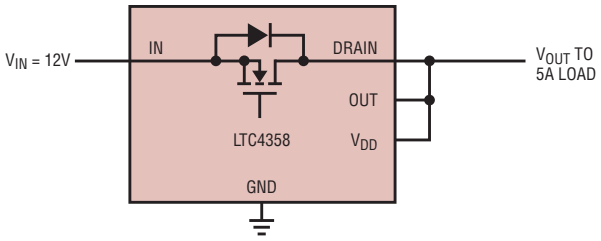
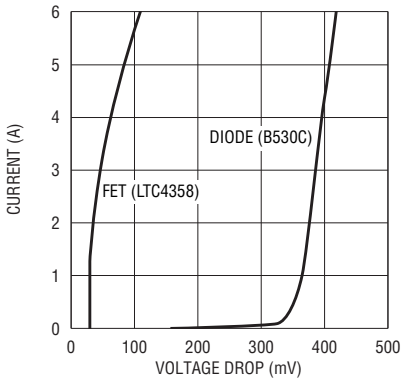


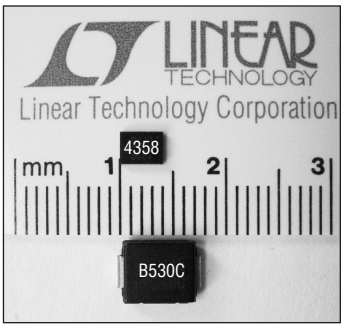
Figure 1. No external components are needed for a 12V/5A ideal diode.

With one-fourth the dissipated power, system efficiency is increased and PCB layout is simplified—no need for costly and bulky heat sinks.

Ideal Diode Easier to Use Than a Schottky

Of particular interest is the LTC4358, which includes an internal 20mΩ





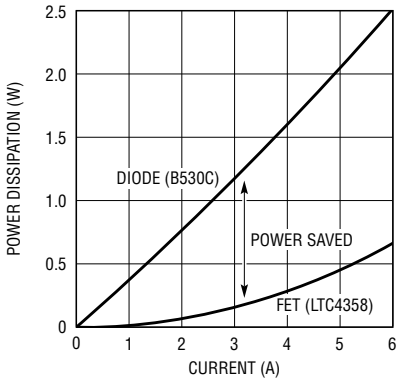


Figure 2. The LTC4358 ideal diode takes on a 5A B530C Schottky diode. The LTC4358 easily wins in voltage drop, power loss and package size.

Table 1. Comparison of ideal diode parts

Part Number	Description	Operating Voltage	Configuration	Package
LTC4355	Positive Voltage Diode-OR Controller and Monitor	9V–80V, 100V Abs Max	Dual, External MOSFETs	DFN14 (4mm × 3mm), SO16
LTC4357	Single Positive Voltage Ideal Diode Controller	9V–80V, 100V Abs Max	Single, External MOSFET	DFN6 (2mm × 3mm), MSOP8
LTC4358	Ideal Diode	9V–26.5V, 28V Abs Max	5A Internal MOSFET	DFN14 (4mm × 3mm), TSSOP16

MOSFET as the pass element. No external components are required. The IN pins are the source of the MOSFET and act like the anode of a diode, while the drain behaves as the cathode, as shown for a 12V/5A application in Figure 1. When power is first applied, the load current initially flows through the MOSFET's body diode. The MOSFET's gate is enhanced and turned on to maintain a 25mV forward voltage drop. If the load current causes more than 25mV of voltage drop, the MOSFET is driven fully on, and the forward drop equals $R_{DS(ON)} \bullet I_{LOAD}$. If the load current reverses, as may occur during an input short, the LTC4358 responds by turning off the internal MOSFET in less than 0.5µs.

Power Saved Versus Schottky Diode

Compared to a B530C Schottky diode in the SMC package, not only is the LTC4358's DE14 (4mm × 3mm) package one-fourth the size, the voltage drop and power dissipation are also considerably less as shown in Figure 2. The reduced voltage drop of the ideal diode also increases the voltage at the load, which reduces the capacitance required to hold up the output during supply disruptions. The power dissipated at 5A in the Schottky is 2W versus 0.5W for the LTC4358. With one-fourth the power dissipated, system efficiency is increased and PCB layout is simplified—no need for costly and bulky heat sinks.

Not only is the LTC4358's DE14 (4mm × 3mm) package one-fourth the size, the voltage drop and power dissipation are also considerably less than a Schottky. The reduced voltage drop of the ideal diode also increases the voltage at the load, which reduces the capacitance required to hold up the output during supply disruptions.

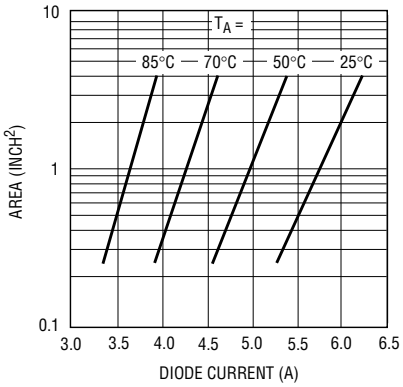


Figure 4. Maximum diode current vs PCB area

PCB Layout

As described above, with only one-fourth as much power dissipation as a Schottky, thermal layout with the LTC4358 is much easier. Most of the heat escapes the part through the DRAIN/exposed pad, while some exits through the IN pins. Maximizing the copper of these connections increases the allowable maximum current. Figure 3 shows an optimal layout for a 1" × 1" single sided PCB with the DFN package. Copper connected to the exposed pad above and below the LTC4358 helps remove heat from the package. If you are using a two-sided PCB, use vias under the LTC4358 to transfer heat to copper on the bottom of the PCB, thus increasing the maximum current by 10%. Use Figure 4 to determine the amount of copper area needed for a specified current and ambient temperature.

Conclusion

The LTC4358 is a MOSFET-based ideal diode that can directly replace a 5A Schottky diode in 9V to 26.5V applications. The LTC4358 betters a Schottky by a factor of four on voltage drop, power loss and package size, thus significantly shrinking the thermal layout and improving overall performance. Also, simple optimization the PCB layout increases the maximum current—no heat sinks required.

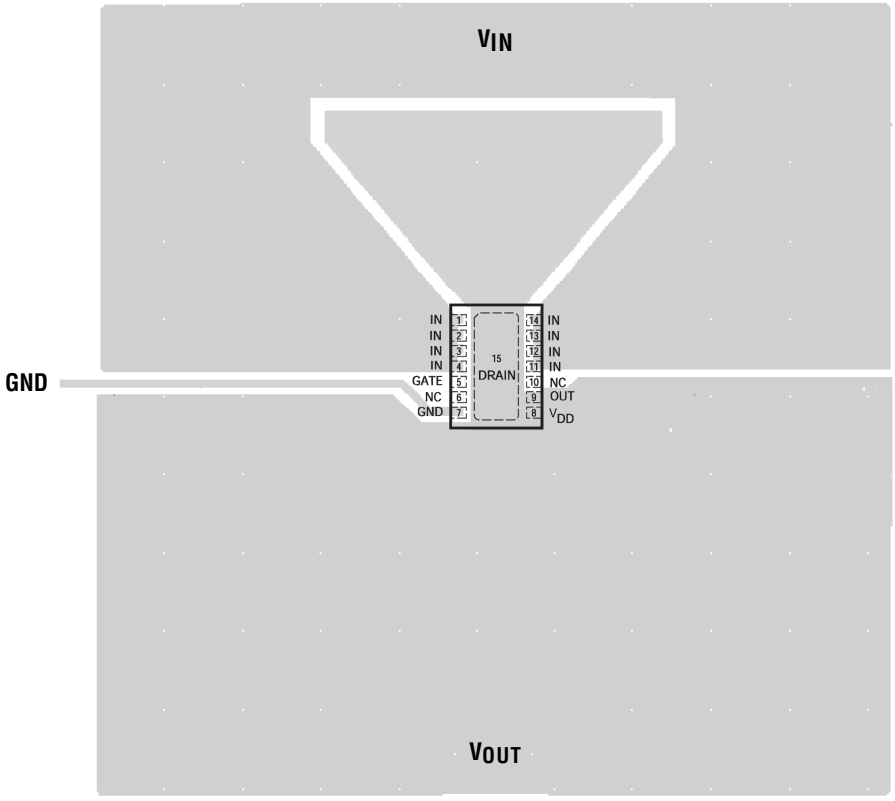


Figure 3. DFN layout considerations for 1" × 1" single sided PCB

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6mm × 6mm DC/DC Controller Regulates Three Outputs; or Combine Two Outputs for Twice the Current

by Theo Phillips

Introduction

The LTC3853 is a versatile 3-phase synchronous buck controller with on-chip drivers in a 6mm × 6mm QFN package. While each channel can independently deliver currents in excess of 15A, two of the channels can be combined for twice the current, with their relative operating phase automatically optimized to reduce output ripple. Channels 1 and 2 can be programmed for outputs from 0.8V to 5V, while channel 3 can support outputs from 0.8V to 13.2V.

Multiphase Operation

The LTC3853 can be configured for three single phase outputs, or for two outputs with channels 1 and 2 tied together. In a 3-output setup, the switches operate 120° out of phase, reducing the input RMS ripple current and minimizing the input capacitance requirement.

Dual Output Converter with 2 + 1 Operation

Figure 1 shows a 2-output converter working from a 14V to 24V input. Channels 1 and 2 feed the same 1.8V output, while channel 3 controls a second 12V output. This 2 + 1 mode requires just one RUN pin (RUN1) to enable both channels 1 and 2. The error amp of channel 2 is disabled and both channels share channel 1's feedback divider. Post package trimming of the current sense comparators provides excellent current sharing between channels 1 and 2, as the load step of Figure 2 shows. Channels 1 and 2 run 180° out of phase to minimize the output ripple on their 2-phase single output. A minimum on-time of <90 nanoseconds allows low duty cycle operation even at high frequencies—at $24V_{IN}$ to $1.8V_{OUT}$, this 500kHz regulator never misses a pulse.

The $EXTV_{CC}$ pin can be connected to a 5V supply to power the internal MOSFET drivers and control circuits. An internal switch connects $EXTV_{CC}$ to $INTV_{CC}$ with a typical voltage drop of just 50mV. If $EXTV_{CC}$ is not connected, the LTC3853's internal regulator uses the main input supply, V_{IN}, to provide 5V to the internal circuitry and drivers at $INTV_{CC}$. In either case, the switching frequency is set with a divider from the predictable 5V at $INTV_{CC}$, with 1.2V at the FREQ pin corresponding to free-running 500kHz. If an external frequency source is available, a phase locked loop enables the LTC3853 to

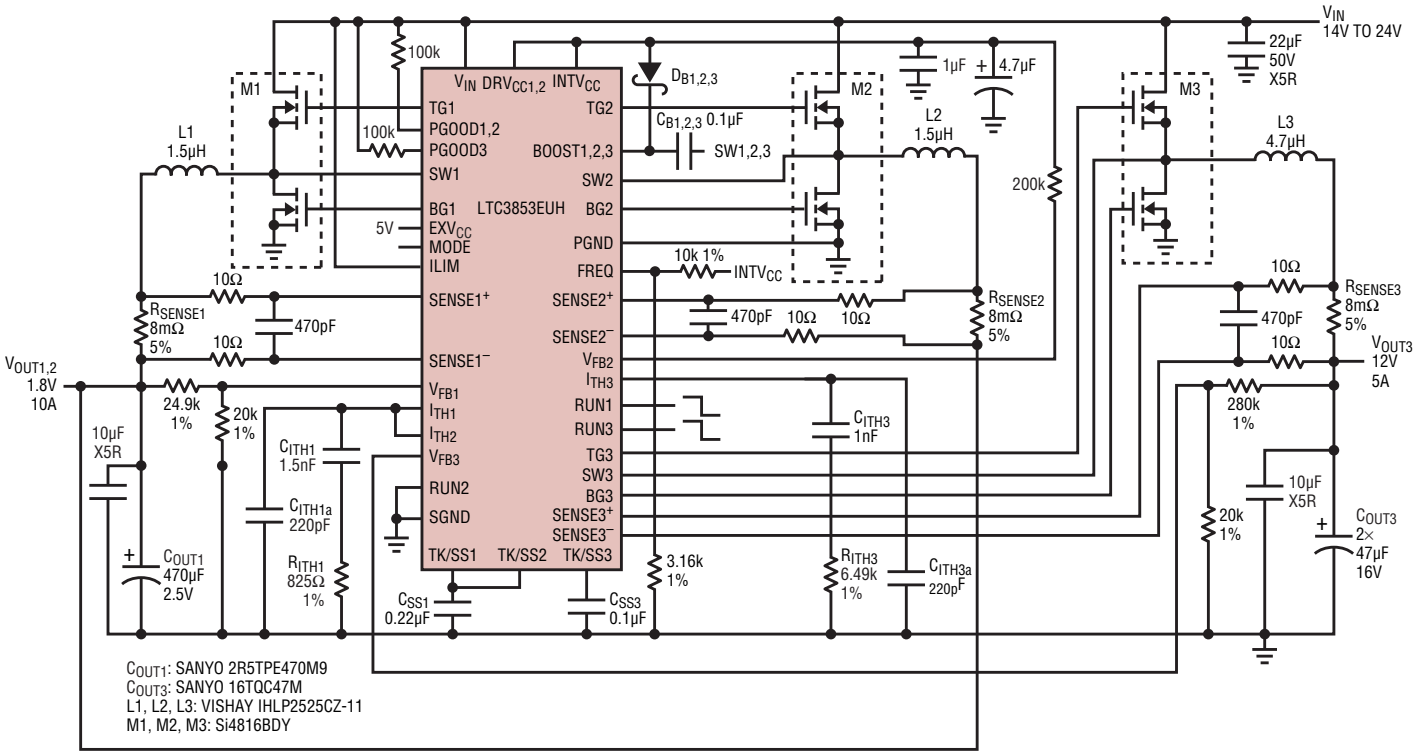

Figure 1. For applications that need up to 30A of current, channels 1 and 2 of the LTC3853 can be combined to share the load for a single output. The two channels operate 180º out of phase to minimize output ripple. Channel 3's high common mode range allows it to provide 12V.

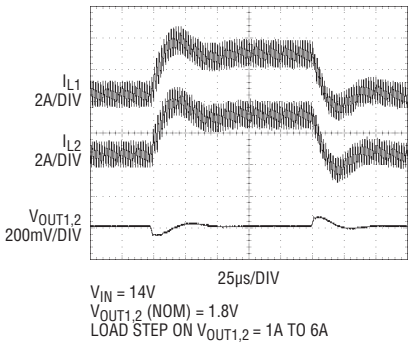

Figure 2. Post-package trimming of the LTC3853's current sense comparators provides excellent current sharing between channels 1 and 2, even during a transient.

sync with frequencies between 250kHz and 750kHz.

The LTC3853 can be set to operate in one of three modes under light load conditions. Burst Mode operation offers the highest light load efficiency by switching in a "burst" of one to several pulses replenishing the charge stored in the output capacitors, followed by a long sleep period when the load current is supplied by the output capacitors. Forced continuous mode offers fixed frequency operation from no load to full load, providing the lowest output voltage ripple at the cost of light load efficiency. Pulse-skipping mode operates by preventing inductor current reversal by turning off the synchronous switch as needed. This mode is a compromise between the other two modes, offering lower ripple than Burst Mode operation and better light load efficiency than forced continuous mode. Regardless of the mode selected, the LTC3853 operates in constant frequency mode at higher load currents. Figure 3 shows the efficiency in each of the three modes.

Each of the LTC3853's channels can be enabled with its own RUN pin, or slewed up or down with its own TRACK/SS pin. Tracking holds the feedback voltage to the lesser of the internal reference voltage or the voltage on TRACK/SS, which can be brought up with an external ramp or with its own 1.2µA internal current source. With all of the TRACK/SS pins held low and any output enabled through its RUN pin, the 5V $INTV_{CC}$ is still available for ancillary keep-alive circuits.

Pulse-skipping mode is always enabled at start-up to prevent sinking current from a pre-biased output voltage. When the output reaches 80% of the set value, the part switches over to forced continuous mode until the output has entered the POWER GOOD window, at which point it switches over to the selected mode of operation. Forced continuous mode reduces the output ripple as the power good threshold is crossed, to ensure that the POWER GOOD indicators make just one low to high transition.

Three different max current comparator sense thresholds can be set via the ILIM pin. The current is sensed using a high speed rail-to-rail differential current sense comparator. The circuit of Figure 1 uses accurate sense resistors between the inductors and the outputs. For reduced power loss at high load currents, the LTC3853 can also monitor the parasitic resistance of the inductor (DCR sensing). Peak inductor current is limited on a cycle-by-cycle basis and is independent of duty cycle. If load current is high enough to cause the feedback voltage

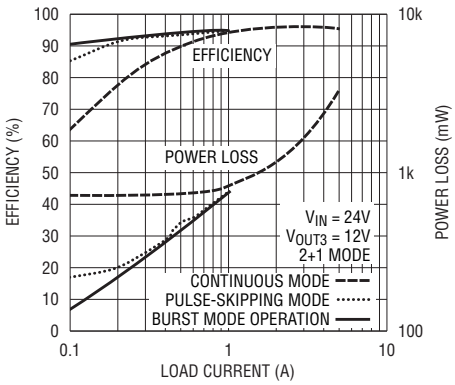

Figure 3. Efficiency for channel 3 in Figure 1—in each of the three modes of operation

to drop, current limit fold back protects the power components by reducing the current limit. For predictable tracking, current limit fold back is disabled during start-up. Input undervoltage lockout, output overvoltage shutdown and thermal shutdown also protect the power components and the IC from damage.

Conclusion

The LTC3853's small footprint belies its versatility and extensive feature set. From inputs up to 24V it can regulate three separate outputs, or it can be configured for higher currents by tying channels 1 and 2 together. Either way, the phase relationship between channels is automatically optimized to reduce ripple currents. At low duty cycles, the short minimum on-time ensures constant frequency operation, and peak current limit remains constant even as duty cycle changes. The cost-effective LTC3853 incorporates these features, and more, into a 40-pin 6mm × 6mm QFN package.

LT3570, continued from page 29

DSL Modem

Figure 4 shows an application for a DSL modem or set-top box. The supply voltage for V_{IN2} comes from a wall adapter that can range from 8V to 30V. This voltage is stepped down to 5V at 100mA for V_{OUT2}, which then supplies the power to drive both the boost regulator and LDO controller. V_{OUT1} is set to 8V at 200mA and V_{OUT3} is set to 3.3V at 500mA. Figure 5 shows the load step response of V_{OUT1} and V_{OUT2} with a 200mA load step on V_{OUT1}.

Conclusion

The LT3570 is a monolithic dual output switching regulator (buck and boost) with a NPN LDO controller and is ideal for a broad variety of applications. Because the LT3570 offers a high level of system integration, it greatly simplifies board design for complex applications that need multiple voltage supply rails. With the flexibility of independent supply inputs and adjustable frequency, the user can set a wide array of custom output voltages. The LT3570 is a feature rich solution that satisfies the needs for multiple output voltages in a compact solution.

New Device Cameos

Dual 8A or Single 16A Step-Down DC/DC µModule Regulator in a 15mm × 15mm Surface Mount Package

The LTM4616 is a complete dual DC/DC µModule regulator system in a tiny surface mount package. The LTM4616 can regulate either two voltages ranging from 0.6V to 5V at up to 8A each, or one output voltage at up to 16A by sharing current from each output in a multiphase configuration.

The LTM4616's versatility is extended by its ability to operate from either two different input supply rails ranging from 2.375V to 5.5V (6V max) or from one input supply by tying the input pins together. This complete DC/DC system solution includes all the support components needed for a dual point-of-load regulator: inductors, capacitors, DC/DC controller, compensation circuitry and power switches. All are encapsulated and protected within a plastic surface mount LGA (land grid array) package. The package dimensions are 15mm × 15mm with a height of only 2.8mm, providing a low profile point-of-load regulator that allows smooth air flow for cooling in densely populated circuit boards. It is also a simple solution for powering both core and I/O supplies for FPGAs and ASICs.

The LTM4616 is guaranteed to have only ±1.75% total DC output error over the full operating temperature range, including the line and load regulation. As a current mode device with high switching frequency, the LTM4616 has a very fast transient response to line and load changes while operating with excellent stability with a variety of output capacitors, including all ceramic capacitors. Efficiency is as high as 94%. The device supports frequency synchronization, multiphase operation, spread spectrum phase modulation, output voltage tracking and margining. Safety features include overvoltage and overcurrent protection as well as thermal shutdown.

Monolithic Linear USB Battery Charger with High Efficiency Buck-Boost and Buck Converters

The LTC3558 is an efficient, multifunction power management solution for handheld applications. The LTC3558 integrates a stand-alone Li-Ion/Polymer battery charger and two high efficiency synchronous regulators—one buck-boost and one buck—in a compact low profile 3mm × 3mm QFN package. The linear battery charger can deliver up to 950mA charge current from a wall adapter supply, or up to 500mA charge current from a USB port. The LTC3558's standalone autonomous operation simplifies design, eliminating the need for an external microprocessor for charge termination. Both switching regulators are designed to operate over the Li-Ion/Polymer range of 2.7V to 4.2V while delivering output currents up to 400mA each.

The LTC3558's integrated synchronous buck regulator features 100% duty cycle operation, while the buck-boost regulator is capable of regulating its programmed output voltage (typically 3.3V) over the entire Li-Ion/Polymer operating range. The integrated low $R_{DS(ON)}$ switches enable efficiencies as high as 92%, maximizing battery run time. In addition, Burst Mode operation optimizes efficiency at light loads with a quiescent current of only 20µA for the buck-boost and 35µA for the buck (less than 1µA in shutdown for each). The high 2.25MHz switching frequency allows the utilization of tiny low cost capacitors and inductors less than 1mm in height. Furthermore, the regulators are stable with ceramic output capacitors, achieving very low output voltage ripple.

The LTC3558's battery charger contains a high degree of USB functionality, including 20%/100% full-scale charge current setting, an SUSP pin for shutdown/enable, and 4 different indication states on the $\overline{CHRG}$ pin.

12-Bit, 3Msps SAR ADC Dissipates Only 7.2mW in Tiny TSOT-23 Package

The LTC2366 is a 12-bit successive approximation register (SAR) ADC that outputs data at up to 3Msps in tiny 6- and 8-lead TSOT-23 packages. Operating from a single 2.35V to 3.6V supply, the LTC2366 consumes only 7.2mW at the maximum output rate, a 20% power savings over the nearest competitor. With its tiny footprint and very low power dissipation, the LTC2366 is ideal for a wide variety of portable and space-constrained applications, including medical devices, communication systems, and industrial monitors.

The LTC2366 is Linear's fastest offering in a family of five TSOT-23 pin- and software-compatible ADCs. The LTC2365 output data rate is guaranteed up to 1Msps and the LTC2362 up to 500ksps. For lower speeds, the LTC2361 is guaranteed up to 250ksps and the LTC2360 up to 100ksps. Power is optimized for each sample rate, as the LTC2360 draws just 1.5mW at 100ksps. Power dissipation can be further decreased with a shutdown mode that reduces the supply current to 2µA (max), saving battery life. All five ADCs are offered in industry standard 6-pin TSOT-23 packages, as well as 8-pin TSOT-23 packages that include an external reference pin and a digital output supply pin (OVDD) that can range between 1V and VDD. The LTC2366, LTC2365, LTC2362, LTC2361, and LTC2360 can be used for monitoring precision DC or AC signals in a variety of applications, including automotive.

These ADCs Communicate via a serial SPI/QSPI/Microwire-compatible interface with no data latency and achieve excellent DC specifications of ±1LSB INL and ±1LSB DNL. These converters also excel when digitizing AC signals. The LTC2366 measures 72dB SNR, –80dB THD, and 82dB SFDR at a 1MHz input frequency.

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